The CS6804 multi-source MPEG-2 transport stream demux is designed for a broad range of system applications requiring the demultiplexing of data carried over the MPEG-2 transport stream multiplex. This application specific silicon core is capable of demultiplexing four transport streams simultaneously and is ideally suited for integration into next generation, versatile set-top box applications. The CS6804 demux can be customized for specific applications and made available in ASIC or FPGA netlists that have been hand crafted by Amphion for optimal performance while minimizing power consumption and silicon area.

**Figure 1: Amphion Multi Source Transport Stream Demux - Block Diagram**

**TS DEMUX KEY FEATURES**
- Supports four transport stream inputs from independent sources
- PID filtering:
  - PID lookup for up to 64 PIDs
  - Fully host configurable
- Calculation of Program Clock Reference for clock recovery hardware
- Supports up to four video and four audio elementary streams per input source
- CRC carried out on PSI sections in hardware
- Host interface to system RAM for storage and interpretation of:
  - PSI sections
  - Adaptation data
  - Packet Header data
- Input Data Rate:
  - Total Input Maximum: 800Mbps
  - Maximum on one input channel: 300Mbps

**BENEFITS**
- Can support combined MPEG2/4/7 streams
- Flexibility to achieve system performance/power/cost goals
- Can be customized to suit individual applications

**APPLICATIONS**
- Next generation digital cable and satellite set-top box.
- Multi-source personal digital video recorders
- DVD
- Broadband communications
CS6804 FUNCTIONAL DESCRIPTION

The CS6804 accepts transport stream packets in byte-aligned bytes from system front end (FEC decoders) or similar sources. The core interfaces with a host processor via an AMBA host interface to allow the setting of up to 64 PID filters. The core parses out the video and audio Packetized Elementary Stream (PES) packets for selected PIDs for further decoding. This enables quick integration into simple decoders which require easy access to the video and audio PES packets. Where more control is required, the core stores PSI sections, adaptation data and header data in queues in system memory for interpretation by the host processor. This allows the system to quickly get access to the PES data while enabling straightforward customization to the individual application. A Cyclic Redundancy Check (CRC) is carried out on the PSI sections within the core as they are parsed out and stored in system memory. If an error is found then a flag is set to notify the host of this. The Program Check Reference (PCR) carried in the adaptation field is calculated within the core and output for direct use by clock recovery hardware.

FUNCTIONAL BLOCK OVERVIEW

Input FIFOs

There are four Asynchronous Input FIFOs. They provide a bridge between the clock domain of the input and of the core itself. This allows a direct interface to the output of the FEC decoders in a system front end (e.g. in a set top box).

PID Match Units

Each of the 64 PID Match units stores a PID value and descriptor value as defined by the host processor. The PID source number is also written in by the host processor. The PID Match units are used to filter for useful PIDs within the transport stream. Once a valid packet is processed within the TS Parser, the PID number is parsed out and compared to the contents of each of the match units. A match will occur when the source number and PID number equal the respective values stored in the PID Match unit. If a match is found, a Match signal is set high and the index to the matching PID Match unit is determined. The rest of the packet is parsed and any payload is sent to the appropriate FIFO. The output FIFO is selected depending on the Descriptor register in the corresponding PID Match unit.

Transport Stream Parser

The payload is separated from the packet header and adaptation field if present. The parser extracts data from packets of a PID that it has been programmed to recognize. The PID Match unit indicates when this match condition occurs and what sort of stream the packet belongs to so that it can be parsed according to its type. The data is then either parsed into system memory for further interpretation (in the case of PSI or adaptation data) or parsed out for buffering and consumption by PES parsers.

Up to four video streams and four audio streams can be handled by the parser per input source. Context switching occurs between the four input sources and is carried out at byte level so as to preserve the timing and recovery of the PCR for each program in each source.

Host Interface and Memory Structure

The host interface allows control of which PIDs are required and hence which packets will be parsed. Setting up the 64 entry PID match unit allows this filtering at the PID level.

PSI sections, the adaptation field and packet header info can be written to system memory at set locations determined by the core. Each stored PID has a queue associated with it and the position and organization of these queues is managed by the core. The memory required is 32Mbytes in size and is aligned on a 32Mbyte boundary. This memory can be located anywhere within the overall system memory as the host processor generates the offset for the addresses. In this way, the host can interrogate the control registers for the queues to identify the location of the required data and hence enable host parsing of the tables and adaptation fields if required.
SYSTEM DIAGRAM

Figure 2 shows an example system with four transport streams from four separate sources. The PES output can be parsed using PES parsers and input into a multi-stream video decoder such as Amphion’s CS6652 to decode two MPEG-2 video streams (or the CS6654 for decoding four MPEG-2 video streams). The outputs from the decoder are then encoded for PAL/NTSC display. A similar flow is shown for the audio components in the transport streams.

Figure 2: Example System Featuring the CS6804 Transport Demux
ABOUT AMPHION
Amphion (formerly Integrated Silicon Systems) is the leading supplier of speech coding, video/image processing and channel coding application specific silicon cores for system-on-a-chip (SoC) solutions in the broadband, wireless, and multimedia markets.

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