The P2800 2K x 64bit Multi-port Content Addressable Memory (CAM) is designed for address filtering, routing and translation applications in Ethernet, Token Ring, SMDS and ATM systems where high speed operation is necessary. The P2800 will operate up to and beyond the OC-12 data rate of 622MBits s⁻¹. The architecture of the P2800 makes high-speed operation possible through pipelining and interleaving.

**FEATURES**
- 2K x 64bit Content Addressable Memory
- 50ns Compare cycle time
- 15ns Register Read/Write cycle time
- Configurable into areas of CAM and RAM on 16-bit boundaries
- One Parallel Port with full 64bit-wide I/O interface configurable for 16-, 32- or 64-bit operation
- Two Serial Ports configurable for 1-, 4- or 8-bit operation
- Synchronization between Parallel and Serial Ports
- Direct hardware control through Control Bus
- Two 64-bit Comparand Registers
- Four 64-bit Mask Registers
- Two Match Address Registers
- Two Match Data Registers
- Configuration Register
- Next Free Address Register
- Priority Encoder to resolve multiple matches
- Data validity control per location

**Fig.1 Pin connections - top view**
- Support for list entry aging
- Simple Vertical cascading using daisy chain scheme
- Support for 802.3 to/from 802.5 mapping on all ports
- High-speed pipelined and interleaved operation
- 5 Volt I/O operation
- CMOS Technology
- Packaged in a 208-pin flatpack
## ELECTRICAL CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage $V_{CC}$</td>
<td>–0.5 to 7.0 volts</td>
</tr>
<tr>
<td>Supply voltage $V_{dd}$</td>
<td>–0.5 to 4.6 volts</td>
</tr>
<tr>
<td>DC input voltage</td>
<td>–0.5 to $V_{dd} +0.5$ volts</td>
</tr>
<tr>
<td>DC output voltage</td>
<td>–0.5 to $V_{dd} +0.5$ volts</td>
</tr>
<tr>
<td>DC input current</td>
<td>+/-20mA</td>
</tr>
<tr>
<td>DC output current</td>
<td>+/-20mA</td>
</tr>
<tr>
<td>Temperature under bias</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>-55°C to +125°C</td>
</tr>
</tbody>
</table>

### OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>Value</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Operating voltage (periphery)</td>
<td>4.50</td>
<td>5.50</td>
<td>volts</td>
</tr>
<tr>
<td>$V_{dd}$</td>
<td>Operating voltage (core)</td>
<td>3.00</td>
<td>3.60</td>
<td>volts</td>
</tr>
<tr>
<td>VIH</td>
<td>Input voltage logic &quot;1&quot;</td>
<td>2.0</td>
<td>$V_{CC}+0.5$</td>
<td>volts</td>
</tr>
<tr>
<td>VIL</td>
<td>Input voltage logic &quot;0&quot;</td>
<td>–0.50</td>
<td>0.8</td>
<td>volts</td>
</tr>
<tr>
<td>TA</td>
<td>Ambient operating temperature</td>
<td>0</td>
<td>70</td>
<td>°C still air</td>
</tr>
</tbody>
</table>

### ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>Value</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{CC}$</td>
<td>Power supply current periphery</td>
<td>-</td>
<td>TBD</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{CC}(SB)$</td>
<td>Operating voltage (core)</td>
<td>-</td>
<td>TBD</td>
<td>mA /E = HIGH</td>
</tr>
<tr>
<td>$I_{dd}$</td>
<td>Power supply current periphery</td>
<td>-</td>
<td>TBD</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{dd}(SB)$</td>
<td>Operating voltage (core)</td>
<td>-</td>
<td>TBD</td>
<td>mA /E = HIGH</td>
</tr>
<tr>
<td>VOH</td>
<td>Output voltage logic &quot;1&quot;</td>
<td>2.4</td>
<td>-</td>
<td>volts</td>
</tr>
<tr>
<td>VOL</td>
<td>Output voltage logic &quot;0&quot;</td>
<td>-</td>
<td>0.4</td>
<td>volts</td>
</tr>
<tr>
<td>$I_{IIZ}$</td>
<td>Input leakage current</td>
<td>TBD</td>
<td>TBD</td>
<td>µA</td>
</tr>
<tr>
<td>$IOZ$</td>
<td>Output leakage current</td>
<td>TBD</td>
<td>TBD</td>
<td>µA</td>
</tr>
</tbody>
</table>

### CAPACITANCE

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>Value</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{in}$</td>
<td>Input capacitance</td>
<td>-</td>
<td>6.00</td>
<td>pF f=1MHz, $V_{in}$=0V</td>
</tr>
<tr>
<td>$C_{out}$</td>
<td>Output capacitance</td>
<td>-</td>
<td>7.00</td>
<td>pF f=1MHz, $V_{in}$=0V</td>
</tr>
</tbody>
</table>

### AC TEST CONDITIONS

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input signal transactions</td>
<td>0.0 to 3.0 volts</td>
</tr>
<tr>
<td>Input signal rise times</td>
<td>&lt;3ns</td>
</tr>
<tr>
<td>Input signal fall times</td>
<td>&lt;3ns</td>
</tr>
<tr>
<td>Input timing reference</td>
<td>1.5 volts</td>
</tr>
<tr>
<td>Output timing reference</td>
<td>0.8 to 2.4 volts</td>
</tr>
</tbody>
</table>
FUNCTIONAL DESCRIPTION

CAM Array
The CAM Array contains 2K locations that are 64 bits wide. Each location also has two validity bits to indicate Empty, Valid, Temporarily Invalid, and Random Access. Three further bits are included to hold age information for the contents of a location.

The CAM Array can be configured into an area of CAM and an area of RAM across the width of the array on 16-bit boundaries. The CAM section holds associative data while the RAM section holds associated data. Associated data can be accessed as a function of a match in the associated data.

Parallel Port
The Parallel Port is 64 bits wide and provides full bandwidth access into the CAM Array. For architectures that use microprocessors or state machines with narrower data buses, the Parallel Port can be alternatively configured as 16 bits or 32 bits wide; under these circumstances, data is multiplexed on the lower-order bits of the parallel port.

Data is read from and written to the CAM Array and the Register Set via the Parallel Port.

Serial Ports
The Serial Ports operate independently, and can be configured to receive data 1 bit, 4 bits or 8 bits per clock cycle. Data from each Serial Port is assembled in a temporary register ready for transfer into either of the two Comparand Registers.

The amount of data to be assembled from each Serial Port is loaded into a Serial Port Counter which sets a flag when the preset number clock cycles have been received.

Port Synchronization
The Parallel and Serial Ports are synchronized through a handshaking scheme. When the preset count value has been reached by one of the Serial Ports, the flag is set which indicates to the local processor that a value has been assembled and is ready for use. The local processor now transfers that data to one of the Comparand Registers.

The amount of data to be assembled from each Serial Port is loaded into a Serial Port Counter which sets a flag when the preset number clock cycles have been received.

Register Set
The Register Set comprises two Comparand Registers, four Mask Registers, two Match Address Registers, two Match Data Registers, a Configuration Register, and a Next Free Address Register. The Comparand Registers hold the values for comparison. The comparison is masked by a selected Mask Register. Only bits in the Comparand Register that correspond with bits set LOW in the selected Mask Register are compared, other bits are ignored.

Results of comparison are read from the corresponding Match Address Register or Match Data Register. The Match Data Registers provide access to the associated data of the highest-priority matching location. The Next Free Address Register holds the address of the next free location in the device. This information is used for ‘associative’ write cycles to the next free location. The Full Flag daisy chain ensures that write at next free address cycles work globally. The Configuration Register sets up persistent operating conditions within the device.

Control States
Unlike earlier instruction-driven CAM devices, the P2800 is controlled through the hardware Control Bus, leading to single-cycle operation. This approach provides a substantial increase in operating speed.

Control states are input to the P2800 on the Control Bus. These control states divide into four classifications: Read/Write Register, Read/Write Memory, Conditional Write and Compare. The control states give powerful and flexible control over the device.

Match Logic
Results of comparison are indicated through the Match Flag. There is one Match Flag per Comparand Register. In a vertically cascaded system, each Match Flag is fed from one device into Match Input of the next lower-priority device. This connection forms a match daisy chain, allowing match results to be established on a global basis.

Pipelining and Interleaving
The combination of Comparand Register, Match Address Register, Match Data Register and Match Flag Input and Output forms a comparison channel. There are two such channels in the P2800. The data is loaded into the Comparand Register associated with one comparison channel, and comparison is initiated; while the comparison is taking place, results from an earlier comparison in the other comparison channel can be read from the Match Address or Data Register associated with that channel. Therefore, a constant stream of data and results can flow through the device, to provide uninterrupted high-speed operation.

Vertical Cascading
As well as the Match Flag daisy chain, there are daisy chains for both channels of Multiple Match Flags, and a Full Flag daisy chain. All daisy chains operate independently.

Aging
List entry aging is supported through three extra bits per location. A location can be set to age or not, as data is written to the memory. A fully associative aging algorithm is implemented through the control states.
MEMORY MAPPING
The P2800 can be controlled either from a microprocessor or a state machine. In the case of the microprocessor, the wide Control Bus can be driven by using memory mapping. Twelve bits are needed to implement the control states summarised above. Therefore, an address space of 4K locations must be reserved for controlling the P2800. Read or Write cycles to those locations initiate the control state, with data transactions occurring on the DQ0-63 bus. Included in the control states are mask selection, aging control and validity bit control. Note that Read cycles to the Next Free Address output the address on the DQ bus, and can be read by the processor.

VERTICAL CASCADING
Fig. 3 shows a vertically cascaded system of P2800s. Both comparison channels have their own Match Flag and Multiple Match Flag daisy chain. The Match daisy chain prioritizes the individual devices. Global Match, Multiple Match and Full Flags appear from the lowest priority device in the daisy chain. System Match information is fed back up the daisy chain per channel on the /SM0 and /SM1 lines.

PIN DESCRIPTIONS

DQ0-DQ63 (Data Bus, Tri-state, Input/Output, TTL)
The DQ0-DQ63 lines convey data to and from the P2800. When the /E line is HIGH the DQ0-DQ63 lines are held at high impedance. The state of the /W line determines whether the data flow is into or out of the device. The falling edge of /E at the beginning of an Read Cycle causes the data on the DQ0-DQ63 lines to be registered. The source or destination of data on the DQ0-DQ63 lines is determined by the states of the CT0-CT11 lines. The width of the input/output transactions on the DQ0-DQ63 lines is configurable as 16 bits, 32 bits or 64 bits, and is controlled through the Configuration Register. When operating with a bus width of less than 64 bits, the lowest-order bit of a 16- or 32-bit data field is always transmitted via DQ0. The FS0-1 lines determine which field of the internal 64-bit data is accessed by a Read or Write Cycle.

FS0-FS1 (Field Select, Input, TTL)
The FS lines select which field is accessed within the internal 64 data bits during an I/O transaction. The falling edge of /E at the beginning of an Input/Output cycle causes the data on the FS0-FS1 lines to be registered. The mapping from DQ lines to internal data lines is dependent on the configuration of both the Parallel Port and the selected Memory Array organization.

A0-A10 (Address Bus, Input, TTL)
The A0-A10 lines convey addresses to the P2800. During random access Read and Write Cycles, the value presented on them determines the location at which a memory-array transaction occurs. The falling edge of /E at the beginning of an Input/Output cycle causes the data on the A0-A10 lines to be registered.

/ALE (Address Latch Enable, Input, TTL)
The use of the /ALE line is optional, the option being selected in the Configuration Register. The purpose of the Address Latch is to allow common lines to carry information to both the A0-A10 and CT0-CT11 inputs. When address latching is enabled, the /ALE line is used to latch the address value on the A0-A10 lines for cycles that have address information. When the /ALE line is LOW at the beginning of a cycle, the value on the A0-A10 lines is latched into an Address Register at the falling edge of /E, and the Control Bus CT0-CT11 is ignored, therefore the A0-A10 and CT0-CT11 buses can be wired in parallel. Subsequent cycles that specify an address will use the value held in the Address Latch.

/E (Strobe, Input, TTL)
The /E input is the strobe for the P2800. When the /E line is held HIGH the DQ0-DQ63 lines are forced to the high-impedance state, the device is disabled, and static power is consumed. The falling edge of /E is used to register control, address and data inputs at the beginning of a random access or associative cycle.

Fig. 3 Vertically cascaded P2800 system
/CS (Chip Select, Input, TTL)

The /CS input is used to select or deselect a particular device within a vertically cascaded system. When the /CS input is LOW, the P2800 is selected and will be active during the cycle; when the /CS line is HIGH, the P2800 will be deselected and will not be active during the cycle. The Match Flag daisy chain is unaffected by the state of the /CS line: when a device is deselected during a Compare Cycle, the Match Daisy chain passes through that device without being conditioned by it. After the Compare Cycle, the deselected device will behave as if it had a mismatch during the Compare Cycle so that old comparison results may have contained will not upset new comparison results. The state of the /CS line is registered on the falling edge of /E.

/W (Write Enable, Input, TTL)

The /W input selects the direction of data transfer on the DQ0-DQ63 lines during a cycle. It is used in conjunction with the CT0-CT11 lines to define the operation performed by the P2800 during a cycle. The falling edge of /E at the beginning of an input cycle causes the /W line to be registered.

A00-AO10 (Address Output Bus, Tri-state, Output, TTL)

The A00-AO10 lines carry address information from four sources: Comparison Channel 0 Match Address, Comparison Channel 1 Match Address, Address inputs A0-A11, and the Next Free Address Register. The address source is selected with the MAS0-1 lines, and the bus is enabled by the Address enable line, /MAE. In a vertically cascaded system, only the A00-AO10 bus of the highest-priority responding device will be active, all other devices will have their A00-AO10 lines in high impedance state regardless of the condition of the /MAE input.

MAS0-1 (Address Select, Input, TTL)

The MAS0-1 inputs select the source of the address output on the A00-AO10 bus. The possible sources of address are Comparison Channel 0 Match Address, Comparison Channel 1 Match Address, Address inputs A0-A11, and the Next Free Address Register. The address source is selected as follows:

<table>
<thead>
<tr>
<th>MAS0</th>
<th>Address Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Comparison Channel 0 Match Address</td>
</tr>
<tr>
<td>0</td>
<td>Comparison Channel 1 Match Address</td>
</tr>
<tr>
<td>1</td>
<td>Address Inputs A0-A11</td>
</tr>
<tr>
<td>1</td>
<td>Next Free Address Register</td>
</tr>
</tbody>
</table>

/MAE (Match Address Enable, Input, TTL)

The /MAE input controls the impedance of the A00-AO10 bus. When /MAE is LOW the A00-AO10 lines are active; when /MAE is HIGH the A00-AO10 lines are in their high-impedance state. In a vertically cascaded system, only the A00-AO10 bus of the highest-priority responding device will be active, all other devices will have their A00-AO10 lines in high impedance regardless of the condition of the /MAE input.

SA0-SA7, SB0-SB7 (Serial Bus A, B, Input, TTL)

The SA0-SA7 lines convey the serial data to Serial Port SA of the P2800. The data is clocked into Temporary Register TEMPA on the rising edge of the CLKA clock. Data is transferred from TEMPA to either Comparand Register under control of the CT0-CT11 lines. The width of the SA bus is set in the Configuration Register to be 1, 4 or 8 bits. The lowest order bit is always conveyed on the SA0 line. The SB bus is identical to the SA bus with respect to TEMPB and CLKB.

CLKA, CLKB (Serial Clock A, B, Input, TTL)

The CLKA input conveys the clock for Serial Port SA0-SA7. Data on SA0-SA7 is clocked in on the rising edge of CLKA, and the Serial Bit Counter A is also incremented on the rising edge. The serial data is shifted into Temporary Register TEMPA. The number of bits, nibbles or bytes to be clocked in is held in the Configuration Register. After the specified number of bits, nibbles or bytes have been received on Serial Port A, the /ZCA output goes LOW. The rising edge of CLKA is used to synchronize the setting and resetting of /ZCA and the resetting of the Serial Bit Counter for Serial Port SA. Similarly, CLKB clocks the SB bus.

/RST, /RSTB (Reset Serial Input A/B, Input TTL)

The /RSTA bit resets the Serial Bit Counter A to zero when LOW on the rising edge of CLKA. When Serial Bit Counter A is set to zero, /ZCA goes HIGH. /RSTB resets Serial Bit Counter A to zero.

/ZCA, /ZCB (Zero Count A/B, Output TTL)

/ZCA goes HIGH when Serial Bit Counter A is set to zero. /ZCA goes LOW when the Serial bit count is equal to the count value held in the Configuration Register for Serial Port A; it can also be forced HIGH or LOW by a control state on the CT0-CT11 inputs synchronized by the rising edge of CLKA. Serial Bit Counter A is reset to zero by a LOW condition on the /RSTB input at the time of the rising edge of CLKA. /ZCB indicates zero count.

CT0-CT11 (Control Bus, Inputs TTL)

CT0-CT11 are the main control inputs of the P2800. They operate in conjunction with the /W input to determine the state of the DQ bus during an active cycle and the operation performed during that cycle. The CT0-CT11 lines are registered by the falling edge of /E.

/MF0, MF1 (Match Flag 0/1, Output, TTL)

The /MF0 output is the Match Flag for Comparison Channel 0 and indicates whether a valid match has occurred during a Compare Cycle. If there are one or more valid matches in a device, then the /MF0 goes LOW. If the /MI0 line is LOW, then the /MF0 output will go LOW regardless of the match condition in the device. For all other cases the /MF0 output is HIGH. /MF1 is the Match Flag for Comparison Channel 1.
/MI0, /MI1 (Match Input 0, 1, Input, TTL)
The /MI0 input is used in vertically-cascaded systems to prioritize devices for Compare Cycles in Comparison Channel 0. If the /MI0 input is HIGH there is no higher-priority device with a valid match in Comparison Channel 0; the device can then respond to match in its own Memory Array. If the /MI0 input is LOW, then there is a higher-priority device with a valid match in Comparison Channel 0; the device will then not respond to a match in its own Memory Array, although its /MF0 flag will be set LOW indicating a match in Comparison Channel 0 within the CAM system. Similarly, /MI1 prioritizes devices for Comparison Channel 1.

/MMF0, /MMF1 (Multiple-match 0, 1, Output, TTL)
The /MMF0 output is the multiple-match flag for Comparison Channel 0 and indicates whether a multiple match has occurred during a Compare Cycle. If there is more than one valid match within a device, the /MMF0 output goes LOW. The /MMF0 output also goes LOW when there is a single match within the device AND the /MI0 input is LOW. The /MMF0 output is forced LOW if the /MMI0 line is LOW, regardless of the match condition in Comparison Channel 0 within the device. Under all other conditions the /MMF0 output is HIGH. Similarly, /MMF1 is the multiple-match flag for Comparison Channel 1.

/MMI0, /MMI1 (Multiple-match Input 0, 1, Input, TTL)
The /MMI0 input is used in vertically-cascaded systems to provide multiple-match information for Comparison Channel 0 throughout the system. If the /MMI0 line is HIGH, there are no multiple matches amongst higher priority devices. If the /MMI0 line is LOW, there are multiple matches amongst higher-priority devices, so the /MMF0 output is forced LOW indicating a multiple match within the CAM system. Similarly, /MMI1 provides the multiple-match information for Comparison Channel 1.

/SM0, /SM1 (System Match 0, 1, Input, TTL)
The /SM0 input is used in a vertically cascaded system to convey the presence or absence of a match in a lower-priority device to higher-priority devices within the system for Comparison Channel 0. The P2800 uses this information for conditional Write Cycles. The signal is fed from the /MF0 output of the lowest-priority device in the system. /SM1 conveys the presence or absence of a match in a lower-priority device for Comparison Channel 1.

/LPD (Lowest Priority Device, Input, TTL)
The /LPD input is used to indicate the lowest priority device in a vertically cascaded system. The /LPD input of the lowest priority device is connected to Ground, the /LPD inputs of all other devices in the system are connected to Vdd. In a single-chip system, the /LPD line must be connected to Ground.

/FF (Full Flag, Output, TTL)
The /FF output is the Full Flag that indicates whether the device is full. If there are one or more empty locations, the /FF output is HIGH; if all locations are full, and the /FI input is LOW, then the /FF goes LOW. In a vertically-cascaded system, the /FF output of a higher-priority device is connected to the /FI input of the next-lower-priority device. If the /FI input is HIGH, the /FF flag will go HIGH regardless of the full condition within the device. The /FF output of the lowest-priority device in a vertically cascaded system represents the system Full Flag.

/FL (Full Input, Input, TTL)
The /FL input is used in vertically-cascaded systems to establish the Full condition within the CAM system. If the /FL input is HIGH for a particular device, there is at least one empty location in a higher-priority device in the system. If the /FL input is LOW for a particular device, then there is no empty location in the higher-priority devices; the device will then condition its own /FF line HIGH if it has any empty locations, or LOW if it does not. The /FL input and /FF output indicate to an individual device within a vertically cascaded system how to respond to a Write-at-next-free-address Cycle when the empty locations are distributed non-contiguously throughout the system.

/RST (Reset, Input, TTL)
This pin provides a hardware reset of the P2800. At power-up this pin must be pulled LOW for the device to initialize. After the /RST line returns HIGH the device will be in the reset condition. Pulling the /RST LOW has the same result as the control code CT11-CT0 = 200H of 201H.

/Vcc (Positive Power Supply +5V)
These pins are the main power supply connections to the P2800. Vcc must be held at +5V ±10% relative to the GND pin for correct operation of the device.

/Vdd (Positive Power Supply +3.3V)
These pins are the auxiliary power supply connections to the P2800. Vdd must be held at +3.3V ±10% relative to the GND pin for correct operation of the device.

/GND (Ground)
The common GND pins, which must be held at 0V, system reference potential, for correct operation of the device.
CONTROL STATE SUMMARY

Register Write Cycles
- DQ0-63 to Comparand Register 0,1
- DQ0-63 to Configuration Register
- DQ0-63 to Mask Register 0,1,2,3
- Reset CAM
- Reset Serial Port A,B
- Match Address to Match Data Register 0,1
- Temporary Register to Comparand Register A,B
- Set Aging Counter

Memory Write Cycles
- Comparand Register 0,1 to Address
- Configuration Register to Address
- DQ0-63 to Address
- DQ0-63 to Next Free Address
- Set Validity/Aging at Address
- Mask Register 0,1,2,3 to Address

Conditional Write Cycles
- If Match 0,1 then Comparand 0,1 to Address
- If No Match 0,1 then Comparand 0,1 to Address
- If Match 0,1 then Set Validity at Address
- If Match 0,1 then Set Validity at All Matching Locs
- If Match 0,1 then Set Age at Highest Prio Match
  else Comparand Register 0,1 to Addr
- If Match 0,1 then Set Age at All Matching Locations
  else Comparand Register 0,1 to Addr

Compare Cycles
- Compare Comparand Register 0,1 with CAM Array
- Compare DQ0-63 with CAM Array

CONTROL INTERFACE

The control interface of the P2800 comprises the /E Strobe line, the /W Write Enable line, the /CS Chip Select line and CT0-CT11 Control inputs. The functions selected by the CT0-CT11 lines divide into the following categories: Read/Write Register, Read/Write Memory, Conditional Write, and Compare. The Write and Compare operations can be masked by any one of the four Mask registers.

The CT0-CT11 inputs are grouped according to the following scheme:

<table>
<thead>
<tr>
<th>FUNCTION</th>
<th>QUALIFYING BITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>CT11</td>
<td>CT10 CT9 CT8 CT7</td>
</tr>
<tr>
<td>CT6</td>
<td>CT5 CT4 CT3 CT2 CT1 CT0</td>
</tr>
</tbody>
</table>

Register Read Cycles
- Comparand Register 0,1 to DQ0-63
- Configuration Register to DQ0-63
- Address Latch to DQ63-0
- Mask Register 0,1,2,3 to DQ0-63
- Match Address Register 0,1 to DQ0-63
- Match Data Register 0,1 to DQ0-63
- Next Free Address Register to DQ0-63

Memory Read Cycles
- Address to Comparand Register 0,1
- Comparand Register 0,1 to Next Free Address
- Address to Configuration Register
- Configuration Register to Next Free Address
- Address to DQ0-63 Read Validity/Aging at Address
- Address to Mask Register 0,1,2,3
- Mask Register 0,1,2,3 to Next Free Address

Conditional Write Cycles
- If Match 0,1 then Comparand 0,1 to Next Free Addr
- If No Match 0,1 then Compnd 0,1 to Next Free Addr
- If Match 0,1 then Comparand 0,1 to Highest Match
- If Match 0,1 then Set Validity at Highest Match
- If Match 0,1 then Set Age at Highest Prio Match
  else Comparand Register 0,1 to Next Free Addr
- If Match 0,1 then Set Age at All Matching Locations
  else Comparand Register 0,1 to Next Free Addr

Compare Cycles
- Compare Aging Bits with CAM Array
- Compare Validity with CAM Array

CT11 - CT6
- Define the function to be executed by the control state.

CT5 - CT0
- Provide qualification to the function and control the following aspects of the control state:
  - Enable/disable/select Masking
  - Set Validity of a location
  - Enable/Disable aging in a location
  - Enable/disable IEEE802.3/5 mapping
  - Select Serial Port data source
  - Suppress conditional writes
  - Control Reset functions

In the following description of the control states, when a data move to the next free address is executed, the entire contents of the Next Free Address Register are output on DQ0-DQ31, and include the Full Flag on DQ31. Similarly, when a Highest Priority Match Address Register is read, on DQ0-DQ31 it includes the System Match flag for the comparison channel on DQ31.
CONTROL STATES

READ/WRITE REGISTER

CT11 - CT6  /W = LOW  /W = HIGH

000 000  DQ>C0  C0>DQ
000 001  DQ>C1  C1>DQ
000 010  DQ>CF  CF>DQ
000 011  RESERVED  AL>DQ
000 100  DQ>M0  M0>DQ
000 101  DQ>M1  M1>DQ
000 110  DQ>M2  M2>DQ
000 111  DQ>M3  M3>DQ
001 000  RST CAM  HA0>DQ
001 001  RST SA/B  HA1>DQ
001 010  AD>HD0  HD0>DQ
001 011  AD>HD1  HD1>DQ
001 100  TMP>C0/1  NF>DQ
001 101  SAC  RAC
001 110  RESERVED  RESERVED
001 111  NOP  NOP

READ/WRITE MEMORY

CT11 - CT6  /W = LOW  /W = HIGH

010 000  C0>[ADDR]  [ADDR]>C0
010 001  RESERVED  [ADDR]>[NFA]
010 010  C1>[ADDR]  [ADDR]>C1
010 011  RESERVED  [C1]>[NFA]
010 100  CF>[ADDR]  [ADDR]>CF
010 101  DQ>[NFA]  CF>[NFA]
010 110  DQ>[ADDR]  [ADDR]>DQ
010 111  SVA[ADDR]  RVA[ADDR]
011 000  M0>[ADDR]  [ADDR]>M0
011 001  RESERVED  [M0]>[NFA]
011 010  M1>[ADDR]  [ADDR]>M1
011 011  RESERVED  [M1]>[NFA]
011 100  M2>[ADDR]  [ADDR]>M2
011 101  RESERVED  [M2]>[NFA]
011 110  M3>[ADDR]  [ADDR]>M3
011 111  RESERVED  [M3]>[NFA]

CONDITIONAL WRITECT

11 - CT6  /W = LOW  /W = HIGH

100 000  //SM0=LOW  CO>[ADDR]  //SM0=LOW  C0>[NFA]
100 001  //SM1=LOW  C1>[ADDR]  //SM1=LOW  C1>[NFA]
100 010  //SM0=HIGH  CO>[ADDR]  //SM0=HIGH  C0>[NFA]
100 011  //SM1=HIGH  C1>[ADDR]  //SM1=HIGH  C1>[NFA]
100 100  //SM0=LOW  SV[ADDR]  //SM0=LOW  CO>[HPM]
100 101  //SM1=LOW  SV[ADDR]  //SM1=LOW  C1>[HPM]
100 110  //SM0=LOW  SV[AML]  //SM0=LOW  SV[HPM]
100 111  //SM1=LOW  SV[AML]  //SM1=LOW  SV[AML]
101 000  //SM0=LOW  SET AG[HPM]  //SM0=LOW  SET AG[HPM]
101 001  //SM1=LOW  SET AG[HPM]  //SM1=LOW  SET AG[HPM]
101 010  //SM0=LOW  SET AG[AML]  //SM0=LOW  SET AG[AML]
101 011  //SM1=LOW  SET AG[AML]  //SM1=LOW  SET AG[AML]

COMPARE

CT11 - CT6  /W = LOW  /W = HIGH

101 100  C0/CAM  AG(0)/CAM
101 101  C1/CAM  AG(1)/CAM
101 110  C0/CAM  AD>HD0  V(0)/CAM
101 111  C1/CAM  AD>HD1  V(1)/CAM
110 000  DQ>C1  C0/CAM  RESERVED
110 001  DQ>C0  C1/CAM  RESERVED
110 010  DQ>C1  C0/CAM:AD>HD0  RESERVED
110 011  DQ>C0  C1/CAM:AD>HD1  RESERVED
110 1XX  RESERVED  RESERVED
111 000  Factory Diagnostics  Factory Diagnostics
111 001  Factory Diagnostics  Factory Diagnostics
111 01X  RESERVED  RESERVED
111 1XX  RESERVED  RESERVED

CONTROL STATE ABBREVIATIONS

ADDR  Address value
AD  Associated Data
AG  Aging Counter value
AML  All Matching Locations
C0, C1  Comparand Register 0, 1
CAM  Associative section of the Memory Array
CF  Configuration Register
DQ  Data Bus
HA0, HA1  Highest-priority Address Register 0, 1
HD0, HD1  Highest-priority-match Data Register 0, 1
HPM  Highest-priority Matching
INC  Increment
M0, M1, M2, M3  Mask Register 0, 1, 2, 3
NFA  Next Free Address
RST  Reset
RAC  Read Aging Counter
RVA  Read Validity/Aging
SAC  Set Aging Counter
SVA  Set Validity/Aging
[]  Contents of location(s)
>  Move to
//  Compare

EXAMPLE CONTROL STATE DETAILS

Write Cycle: Data Bus to Comparand Register 0
Read Cycle: Comparand Register 0 to Data Bus

CT11 - CT0  /W = LOW  /W = HIGH

000 000  mmm avv  DQ>C0  C0>DQ
010 000  0XX  No Mask  Don't Care
100 100  Mask with M0  Don't Care
101 100  Mask with M1  Don't Care
110 110  Mask with M2  Don't Care
111 110  Mask with M3  Don't Care
a 0  No Data Map  No Data Map
1  802.3/5 Map  802.3/5 Map
vv XX  Don't Care  Don't Care

Cycle Type:  Write Cycle: Register Cycle
            Read Cycle: Register Cycle

Description: Move data between Comparand Register 0 and DQ Bus. Direction of transfer determined by /W. IEEE 802.3 to/from IEEE 802.5 data mapping is selected with a. Data written into Comparand Register 0 can be masked by the Mask Register selected by mmm.
<table>
<thead>
<tr>
<th>No.</th>
<th>Symbol</th>
<th>Parameter Describe</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>tELEL1</td>
<td>Register Read/Write Cycle Time</td>
<td>15</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>tELEH1</td>
<td>Strobe LOW Pulse Width (Register)</td>
<td>9</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>tEHEL</td>
<td>Strobe HIGH Pulse Width</td>
<td>4</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>tWVEL</td>
<td>Write Setup to Strobe LOW</td>
<td>5</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>tELWX</td>
<td>Write Hold from Strobe LOW</td>
<td>0</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>tCTVEL</td>
<td>Control Setup to Strobe LOW</td>
<td>5</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>tELCTX</td>
<td>Control Hold from Strobe LOW</td>
<td>0</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>tFSVEL</td>
<td>Field Select Setup to Strobe LOW</td>
<td>5</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>tELFSX</td>
<td>Field Select Hold from Strobe LOW</td>
<td>0</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>tAQVEL</td>
<td>Address Setup to Strobe LOW</td>
<td>5</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>tELAQX</td>
<td>Address Hold from Strobe LOW</td>
<td>0</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>tELQX</td>
<td>Strobe LOW to Outputs Active</td>
<td>1</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>tELQV</td>
<td>Strobe LOW to Data Valid</td>
<td>-</td>
<td>8</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>tEHQZ</td>
<td>Strobe HIGH to Outputs Hi-Z</td>
<td>-</td>
<td>6</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>tDVEH1</td>
<td>Data Setup to Strobe HIGH (Register)</td>
<td>5</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>tEHDX1</td>
<td>Data Hold from Strobe HIGH (Register)</td>
<td>0</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>tELFFV</td>
<td>Strobe LOW to Full Flag Valid</td>
<td>-</td>
<td>35</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>tFIVFFV</td>
<td>Full Input to Full Flag Valid</td>
<td>-</td>
<td>5</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>tCKHCKH</td>
<td>Serial Port Clock Cycle Time</td>
<td>12.5</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>tCKHCKL</td>
<td>Serial Port Clock LOW Pulse Width</td>
<td>4</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>tCKLCKH</td>
<td>Serial Port Clock HIGH Pulse Width</td>
<td>4</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>tSVCKH</td>
<td>Serial Data Setup to Clock HIGH</td>
<td>2</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>tCKHSX</td>
<td>Serial Data Hold from Clock HIGH</td>
<td>2</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>tCKHZCV</td>
<td>Serial Clock HIGH to Zero Count Valid</td>
<td>-</td>
<td>5</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>tRSTLRSTH</td>
<td>Device Reset LOW Pulse Width</td>
<td>TBD</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>tRSTLCKH</td>
<td>Serial Port Reset LOW to Clock Setup</td>
<td>5</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>tELEL2</td>
<td>Memory Read/Write Cycle Time</td>
<td>45</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>tELEH2</td>
<td>Strobe LOW Pulse Width (Memory)</td>
<td>32</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>tELQV2</td>
<td>Strobe LOW to Data Valid (Memory)</td>
<td>-</td>
<td>30</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>tMIVMFV</td>
<td>Match Input Valid to Match Flag Valid</td>
<td>-</td>
<td>3</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>tMIXMFX</td>
<td>Match Input Invalid to Match Flag Invalid</td>
<td>2</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>tELMFV</td>
<td>Match Flag Valid from Compare Cycle</td>
<td>-</td>
<td>50</td>
<td>ns</td>
<td>/M10,1=HIGH</td>
</tr>
<tr>
<td>33</td>
<td>tEHQX</td>
<td>Strobe HIGH to Outputs Invalid</td>
<td>1</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>tCKHHRSTH</td>
<td>Serial Clock HIGH to Reset Hold</td>
<td>2</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>35</td>
<td>tDVEH2</td>
<td>Data Setup to Strobe HIGH (Memory)</td>
<td>15</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>36</td>
<td>tEHDX2</td>
<td>Data Hold from Strobe HIGH (Memory)</td>
<td>0</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>37</td>
<td>tCC1</td>
<td>Comparison Cycle Time</td>
<td>50</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>38</td>
<td>tCC2</td>
<td>Comparison Cycle Time, Composite</td>
<td>70</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>39</td>
<td>tMASAOV</td>
<td>Select Input to Address Out Valid</td>
<td>-</td>
<td>5</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>tMAELAOX</td>
<td>Address Enable LOW to Address Out Active</td>
<td>1</td>
<td>5</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>41</td>
<td>tMAELAOV</td>
<td>Address Enable LOW to Address Out Valid</td>
<td>-</td>
<td>8</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>42</td>
<td>tMAEHAOZ</td>
<td>Address Enable HIGH to Address Out Hi-Z</td>
<td>-</td>
<td>6</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>43</td>
<td>tELAOV</td>
<td>Strobe LOW to Address Out Valid</td>
<td>5</td>
<td>50</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>
TIMING DIAGRAMS

**Fig. 4** Register read cycle, pipelined read cycle

**Fig. 5** Register write cycle, pipelined write cycle
Fig. 6 Memory read cycle

Fig. 7 Memory write cycle
Fig. 8 Serial port write cycle

Fig. 9 Compare cycle
TYPICAL APPLICATION

Fig. 10 shows the P2800 in a typical memory-mapped architecture, controlled from a local microprocessor. The Address Decoder maps the control structure of the P2800 into a 4K block of address space. The control states are then fed from the processor Address Bus into the Control Bus CT0-11 inputs. The remaining address space can be used for RAM, ROM and other memory mapping areas.

The P2800 does not need direct addressing because it can be written associatively, at the next free address. Under these circumstances, the address bus is only used to convey control states to the device, although it does support direct addressing for random access cycles if required.

The comparison channels are selected through the control states, and the results of a comparison cycle remain until a subsequent comparison is executed within that channel.

Fig. 10 Memory mapped P2800 system
PACKAGE DETAILS

Dimensions are shown thus: mm (in). For further package information, please contact your local Customer Service Centre.
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