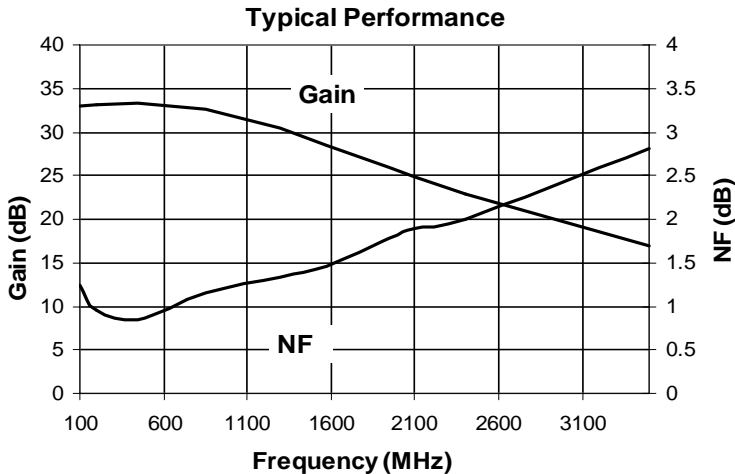




Product Description

The SGL-0622 is a low power, high gain, fully matched LNA designed for 0.1 - 4GHz operation. This LNA is designed for low power, 2.7 to 3.6V battery operation. This amplifier is fully matched and requires only 4-5 external components to achieve 28.5 dB gain at 1.575 GHz and a noise figure of 1.5dB. This RFIC is fabricated using Silicon Germanium technology.

The matte tin finish on Sirenza's lead-free "Z" package is applied using a post annealing process to mitigate tin whisker formation and is RoHS compliant per EU Directive 2002/95. The package body is manufactured with green molding compounds that contain no antimony trioxide or halogenated fire retardants.

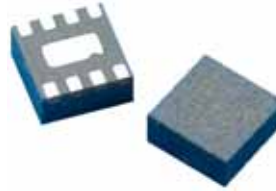


Preliminary

SGL-0622Z



100 - 4000 MHz Low Noise Amplifier Silicon Germanium



Product Features

- Lead Free, RoHS Compliant & Green Package
- High Gain and Low Noise, 28.5dB and 1.5dB respectively @ 1575MHz
- Low Power Consumption, 9mA @ 3.3V
- Fully Matched LNA, only 4-5 external components
- Operates from 2.7 to 3.6V
- Small Package: 2x2 QFN
- High input overdrive capability, +18dBm

Applications

- High Gain GPS Receivers
- ISM & WiMAX LNAs

Symbol	Parameters	Units	Frequency	Min.	Typ.	Max.
S ₂₁	Small Signal Gain	dB	1.575 GHz		28.5	
			2.44 GHz		23	
			3.5 GHz		17	
NF	Noise Figure	dB	1.575 GHz		1.50	
			2.44 GHz		2	
			3.5 GHz		2.8	
P _{1dB}	Output Power at 1dB Compression	dBm	1.575 GHz		5.3	
			2.44 GHz		1.5	
			3.5 GHz		-1.4	
IIP ₃	Input Third Order Intercept Point	dBm	1.575 GHz		-13	
			2.44 GHz		-12	
			3.5 GHz		-8.5	
IRL	Input Return Loss	dB	1.575 GHz		14.3	
			2.44 GHz		12.0	
			3.5 GHz		10.0	
ORL	Output Return Loss	dB	1.575 GHz		9.5	
			2.44 GHz		14.0	
			3.5 GHz		22.0	
S ₁₂	Reverse Isolation	dB	0.05 - 4 GHz		-28	
I _D	Operating Current	mA		7.5	10.5	12.5

Test Conditions: V_{CC} = 3.3V I_D = 10.5mA Typ. IIP₃ Tone Spacing = 1MHz, P_{out} per tone = -15 dBm
T_L = 25°C Z_S = Z_L = 50 Ohms

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Typical RF Performance at Key Operating Frequencies (With Application Circuit)

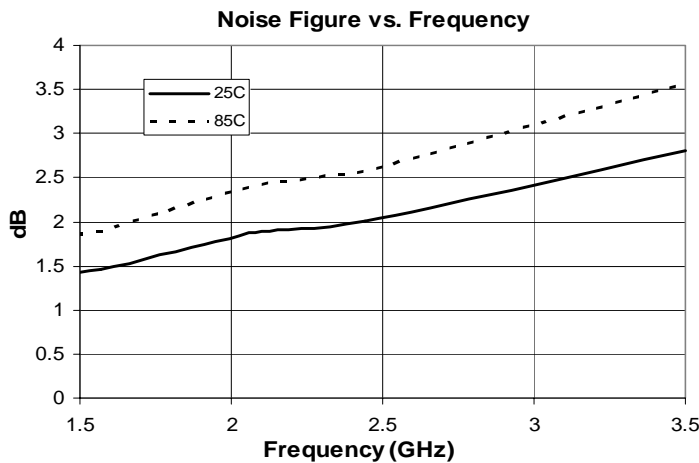
Symbol	Parameter	Unit	Frequency (MHz)							
			100	200	450	850	1575	1950	2440	3500
S ₂₁	Small Signal Gain	dB	34.6	34.9	34.4	32.8	28.5	26.1	23.0	17.0
IIP ₃	Input Third Order Intercept Point	dBm					-13.0		-12.0	-8.5
P _{1dB}	Output at 1dB Compression	dBm					5.3		1.5	-1.4
S ₁₁	Input Return Loss	dB	15.1	20.0	12.6	16.0	14.3	12.8	12.0	10.0
S ₂₂	Output Return Loss	dB	9.2	12.2	11.8	10.4	9.5	12.1	14.0	22.0
S ₁₂	Reverse Isolation	dB	38.8	39.8	38.7	39.9	35.6	34.8	32.0	29.0
NF	Noise Figure	dB	1.25	0.96	0.84	1.16	1.50	1.78	2.01	2.81

Test Conditions: V_{CC} = 3.3V I_D = 10.5 mA Typ. IIP₃ Tone Spacing = 1MHz, P_{out} per tone = -15 dBm
T_L = 25°C Z_S = Z_L = 50 Ohms

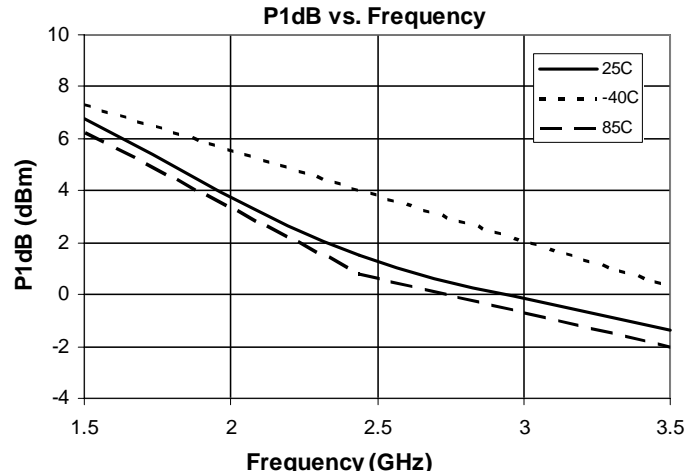
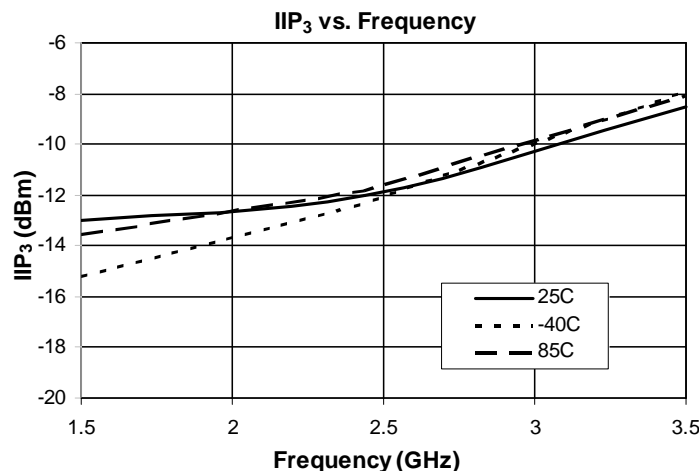
Absolute Maximum Ratings

Reliability & Qualification Information		Parameter	Absolute Limit
	Parameter	Rating	
	ESD Rating - Human Body Model (HBM)	Class 1C	
	Moisture Sensitivity Level	MSL 1	
This product qualification report can be downloaded at www.sirenza.com			
	Max Device Current (I _D)		20mA
	Max Device Voltage (V _D)		4 V
	Max. RF Input Power* (See Note)		+18 dBm
	Max. Junction Temp. (T _J)		+150°C
	Operating Temp. Range (T _L)		-40°C to +85°C
	Max. Storage Temp.		+150°C

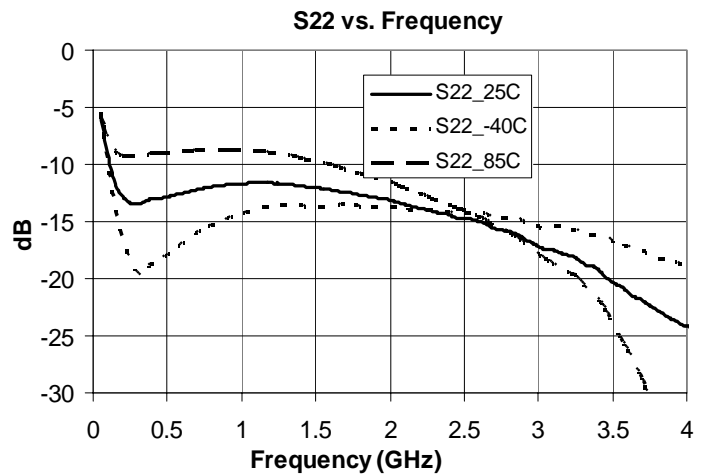
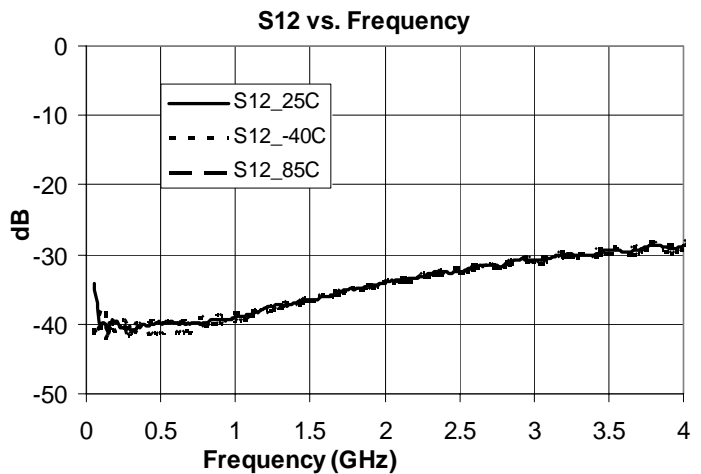
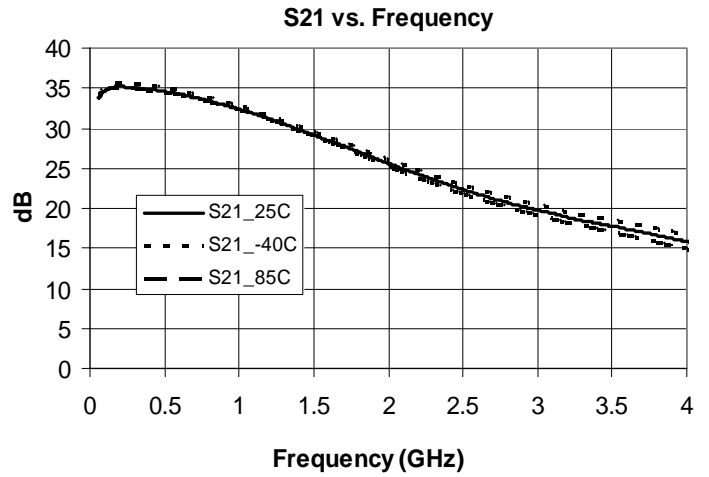
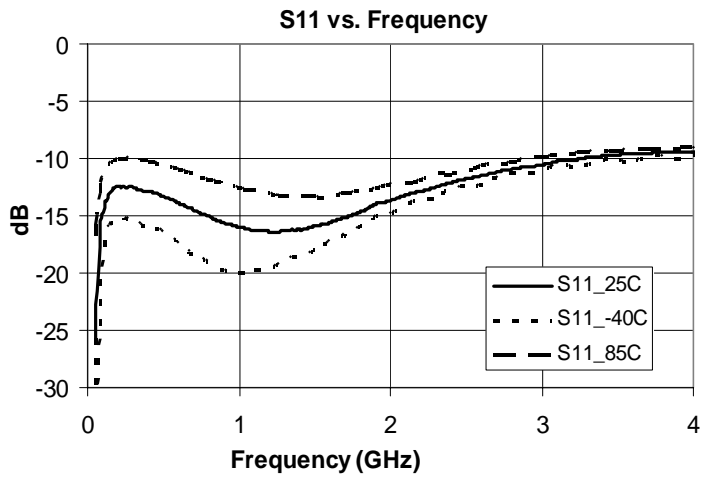
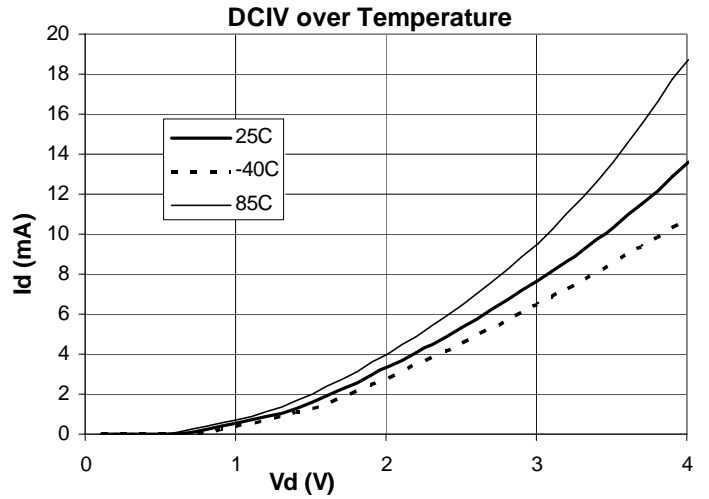
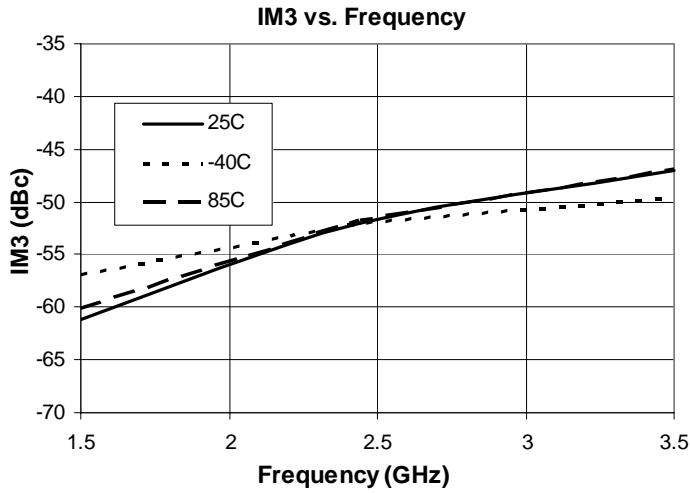
***Note:** Load condition 1, Z_L = 50 Ohms
Load condition 2, Z_L = 10:1 VSWR
Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table on page one.
Bias Conditions should also satisfy the following expression:
 $I_D V_D < (T_J - T_L) / R_{TH, j-l} \quad T_L = T_{LEAD}$



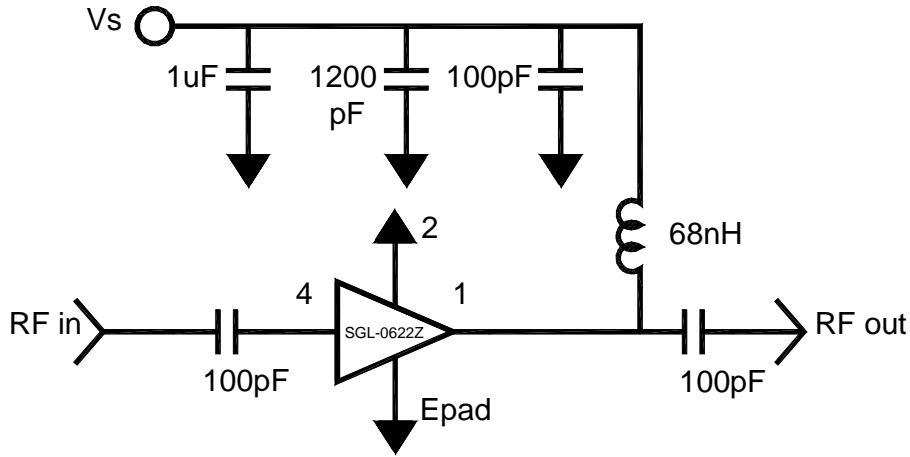
Caution: ESD sensitive
Appropriate precautions in handling, packaging and testing devices must be observed.



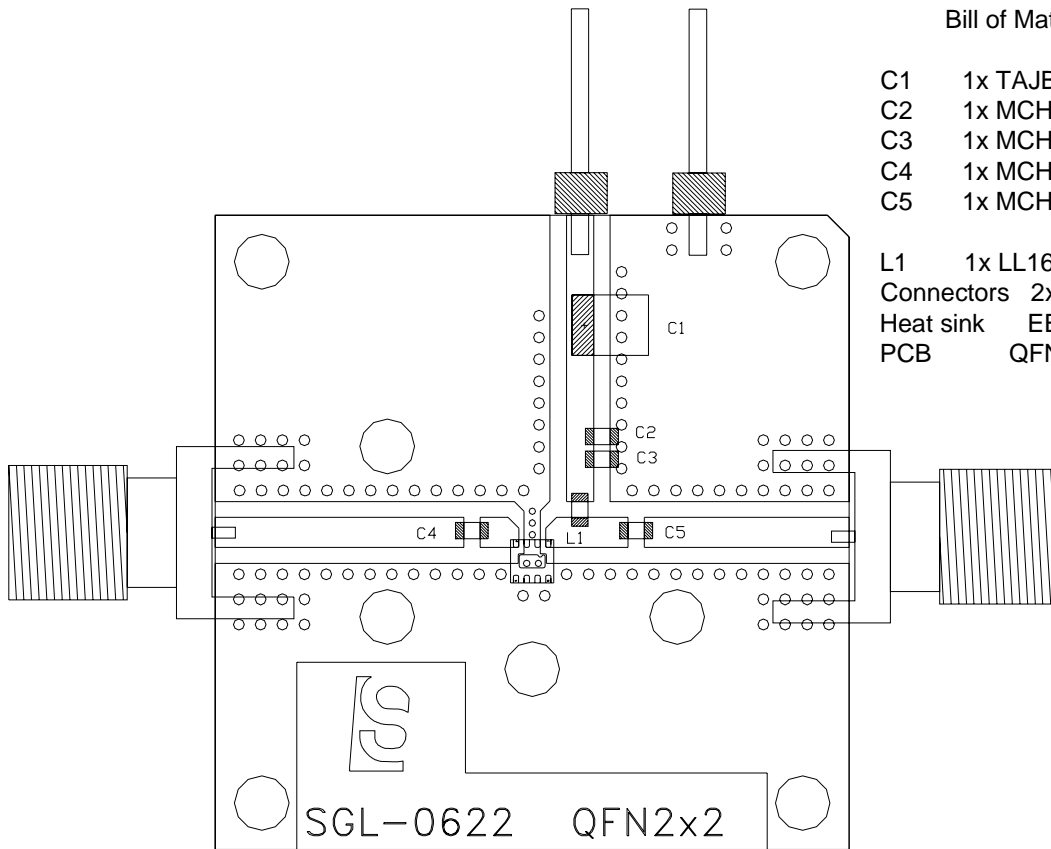
Application Circuit Data, $V_{CC} = 3.3V$, $I_D = 9mA$



Application Schematic



Evaluation Board Layout



Bill of Materials

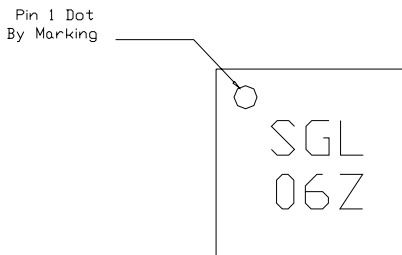
- C1 1x TAJB105KLRH Rohm 1.0uF
- C2 1x MCH185C122KK Rohm 1200pF
- C3 1x MCH185A101JK Rohm 100pF
- C4 1x MCH185A101JK Rohm 100pF
- C5 1x MCH185A101JK Rohm 100pF
- L1 1x LL1608-FS56NJ Toko 68nH
- Connectors 2x PSF-S01-1mm GigaLane Co.
- Heat sink EEF-102059
- PCB QFN2x2

Pin #	Function	Description
1	RF OUT/ V_D	RF output and bias pin. Bias should be supplied to this pin through an external RF choke. (See application circuit)
2	GND	Connect to ground per application circuit drawing.
3,5,6,7,8	N/A	Not Used
4	RF IN	RF input pin. This pin requires the use of an external DC blocking capacitor as shown in the application schematics.
EPAD	GND	Exposed area on the bottom side of the package needs to be soldered to the ground plane of the board for thermal and RF performance. Vias should be located under the EPAD as shown in the recommended land pattern.

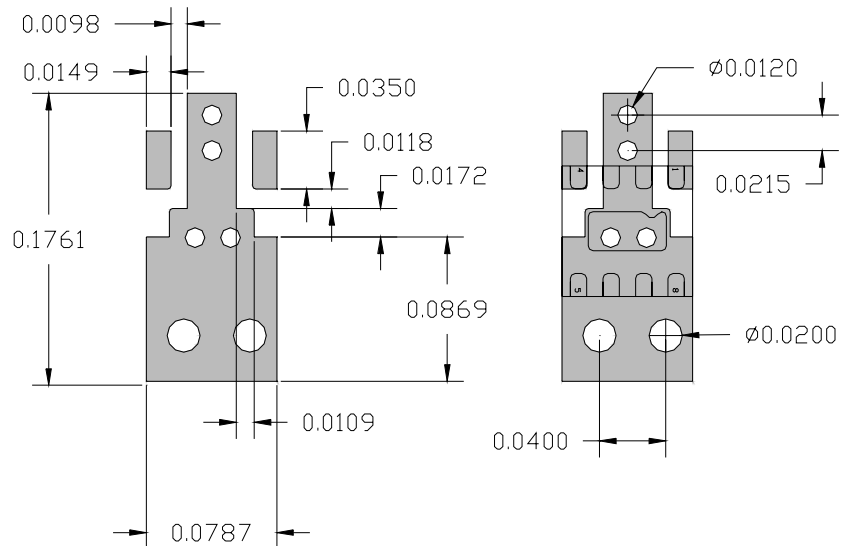
Part Number Ordering Information

Part Number	Reel Size	Devices / Reel
SGL-0622Z	7"	3000

Part Identification



Suggested Pad Layout



Nominal Package Dimensions

Dimensions in inches [millimeters]
Refer to drawing posted at www.sirenza.com for tolerances.

