

BLL6H1214L-250; BLL6H1214LS-250

LDMOS L-band radar power transistor

Rev. 01 — 11 December 2009

Objective data sheet

1. Product profile

1.1 General description

250 W LDMOS power transistor intended for L-band radar applications in the 1.2 GHz to 1.4 GHz range.

Table 1. Test information

Typical RF performance at $T_{case} = 25\text{ }^{\circ}\text{C}$; $t_p = 500\text{ }\mu\text{s}$; $\delta = 20\%$; $I_{Dq} = 100\text{ mA}$; in a class-AB production test circuit.

Mode of operation	f (GHz)	V _{DS} (V)	P _L (W)	G _p (dB)	η_D (%)	t _r (ns)	t _f (ns)
pulsed RF	1.2 to 1.4	50	250	17	55	15	5

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

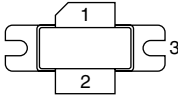
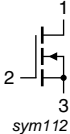
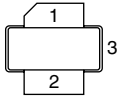
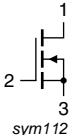
- Typical pulsed RF performance at a frequency of 1.2 GHz to 1.4 GHz, a supply voltage of 50 V, an I_{Dq} of 100 mA, a t_p of 500 μs with δ of 20 %:
 - ◆ Output power = 250 W
 - ◆ Power gain = 17 dB
 - ◆ Efficiency = 55 %
- Easy power control
- Integrated ESD protection
- High flexibility with respect to pulse formats
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (1.2 GHz to 1.4 GHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- L-band power amplifiers for radar applications in the 1.2 GHz to 1.4 GHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLL6H1214L-250 (SOT502A)			
1	drain		 sym112
2	gate		
3	source		
BLL6H1214LS-250 (SOT502B)			
1	drain		 sym112
2	gate		
3	source		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLL6H1214L-250	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A
BLL6H1214LS-250	-	earless flanged LDMOST ceramic package; 2 leads	SOT502B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	100	V
V_{GS}	gate-source voltage		-0.5	+13	V
I_D	drain current		-	72	A
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-c)}$	transient thermal impedance from junction to case	$T_{case} = 85\text{ °C}; P_L = 250\text{ W}$		
		$t_p = 100\text{ }\mu\text{s}; \delta = 10\%$	0.10	K/W
		$t_p = 200\text{ }\mu\text{s}; \delta = 10\%$	0.13	K/W
		$t_p = 500\text{ }\mu\text{s}; \delta = 20\%$	0.15	K/W
		$t_p = 100\text{ }\mu\text{s}; \delta = 20\%$	0.14	K/W

6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ °C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 2.7\text{ mA}$	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 270\text{ mA}$	1.3	1.8	2.2	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}$	-	-	1.4	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	64	72	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	140	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 270\text{ mA}$	3.2	5	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 9.5\text{ A}$	-	50	90	$\text{m}\Omega$

Table 7. RF characteristics

Mode of operation: pulsed RF; $t_p = 500\text{ }\mu\text{s}; \delta = 20\%$; RF performance at $V_{DS} = 50\text{ V}; I_{Dq} = 100\text{ mA}; T_{case} = 25\text{ °C}$; unless otherwise specified, in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_L	output power		250	-	-	W
V_{DS}	drain-source voltage	$P_L = 250\text{ W}$	-	-	50	V
G_p	power gain	$P_L = 250\text{ W}$	15	17	-	dB
RL_{in}	input return loss	$P_L = 250\text{ W}$	-	10	-	dB
$P_{L(1dB)}$	output power at 1 dB gain compression		-	300	-	W
η_D	drain efficiency	$P_L = 250\text{ W}$	50	55	-	%
$P_{droop(pulse)}$	pulse droop power	$P_L = 250\text{ W}$	-	0	0.3	dB
t_r	rise time	$P_L = 250\text{ W}$	-	15	25	ns
t_f	fall time	$P_L = 250\text{ W}$	-	5	25	ns

6.1 Ruggedness in class-AB operation

The BLL6H1214L-250 and BLL6H1214LS-250 are capable of withstanding a load mismatch corresponding to $VSWR = 10 : 1$ through all phases under the following conditions: $V_{DS} = 50\text{ V}; I_{Dq} = 100\text{ mA}; P_L = 250\text{ W}; t_p = 500\text{ }\mu\text{s}; \delta = 20\%$.

7. Application information

7.1 Impedance information

Table 8. Typical impedance
Typical values unless otherwise specified.

f	Z _S	Z _L
GHz	Ω	Ω
1.2	1.268 - j2.623	2.987 - j1.664
1.3	2.193 - j2.457	2.162 - j1.326
1.4	2.359 - j2.052	1.604 - j1.887

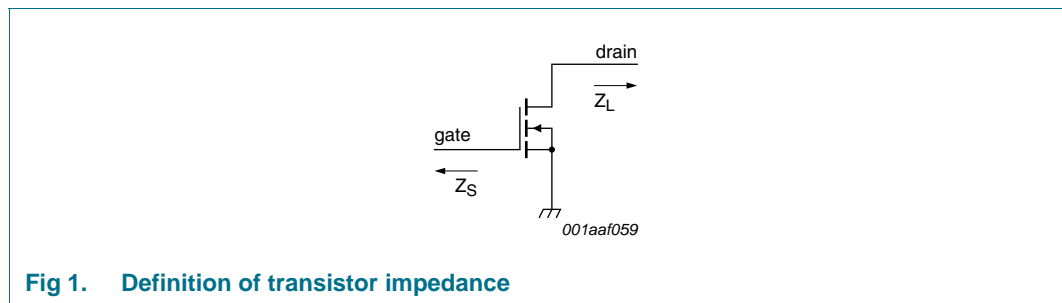
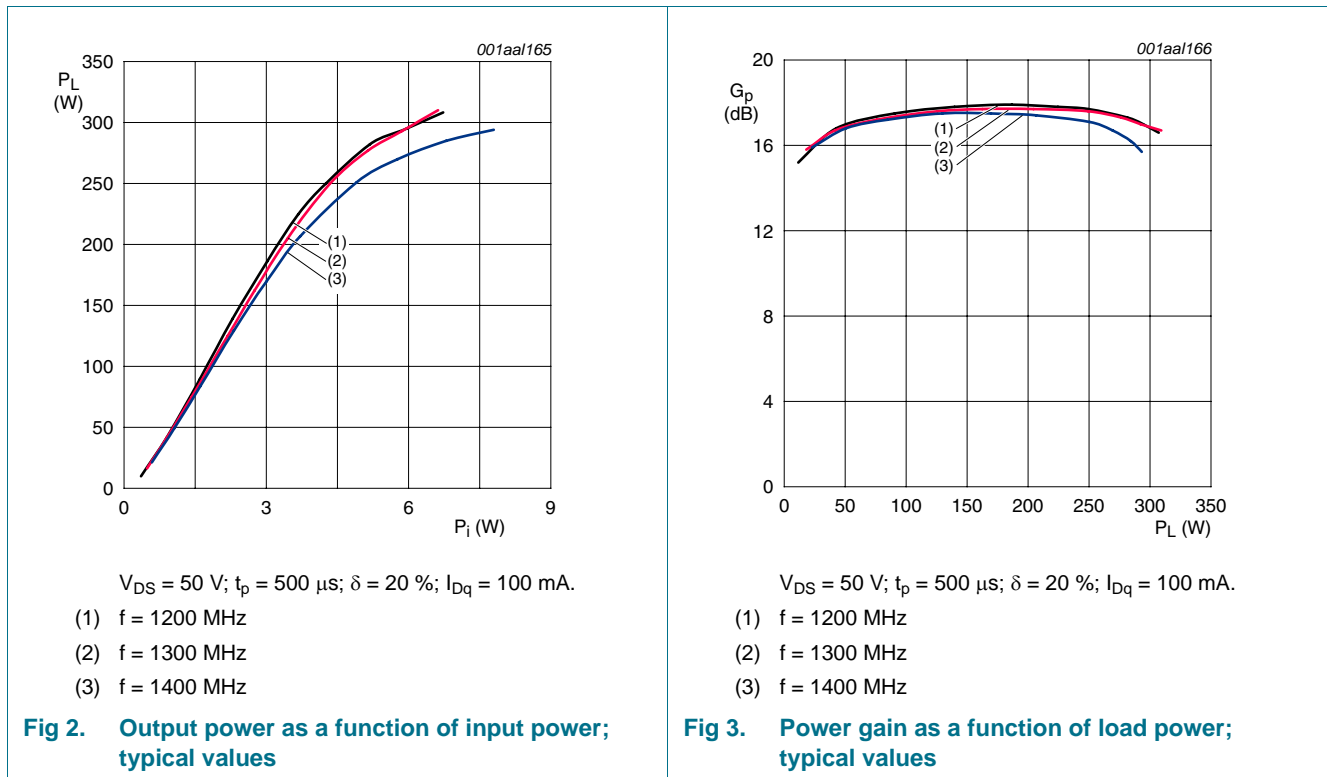
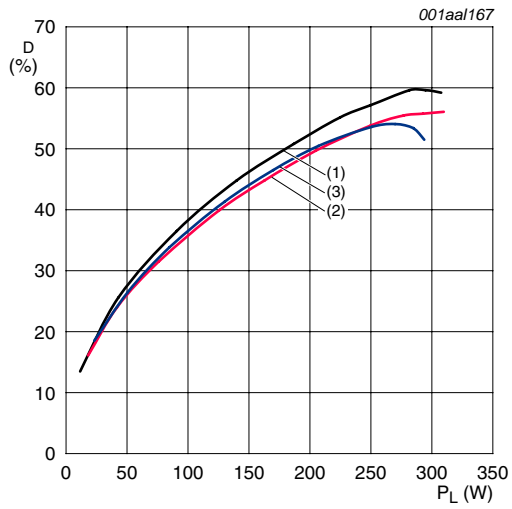


Fig 1. Definition of transistor impedance

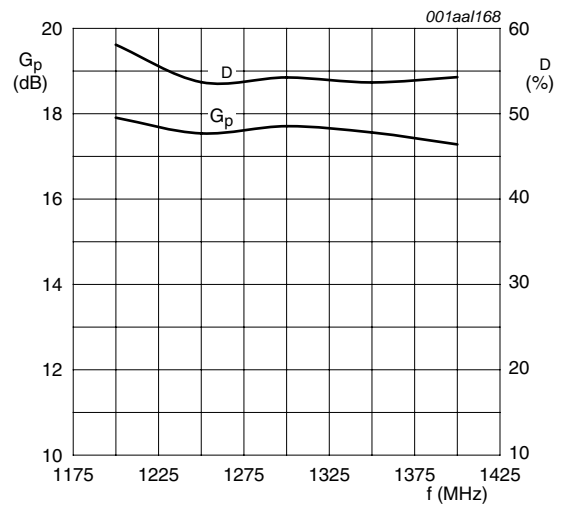
7.2 RF performance





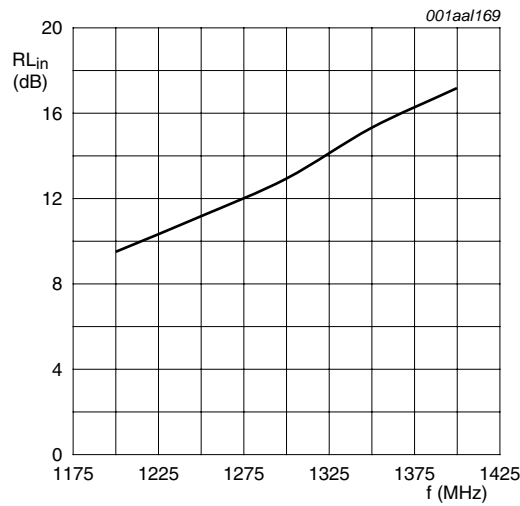
$V_{DS} = 50\text{ V}$; $t_p = 500\ \mu\text{s}$; $\delta = 20\%$; $I_{Dq} = 100\text{ mA}$.
 (1) $f = 1200\text{ MHz}$
 (2) $f = 1300\text{ MHz}$
 (3) $f = 1400\text{ MHz}$

Fig 4. Drain efficiency as a function of load power; typical values



$P_L = 250\text{ W}$; $V_{DS} = 50\text{ V}$; $t_p = 500\ \mu\text{s}$; $\delta = 20\%$; $I_{Dq} = 100\text{ mA}$.

Fig 5. Power gain and drain efficiency as function of frequency; typical values



$P_L = 250\text{ W}$; $V_{DS} = 50\text{ V}$; $t_p = 500\ \mu\text{s}$; $\delta = 20\%$; $I_{Dq} = 100\text{ mA}$.

Fig 6. Input return loss as a function of frequency; typical value

7.3 Application circuit

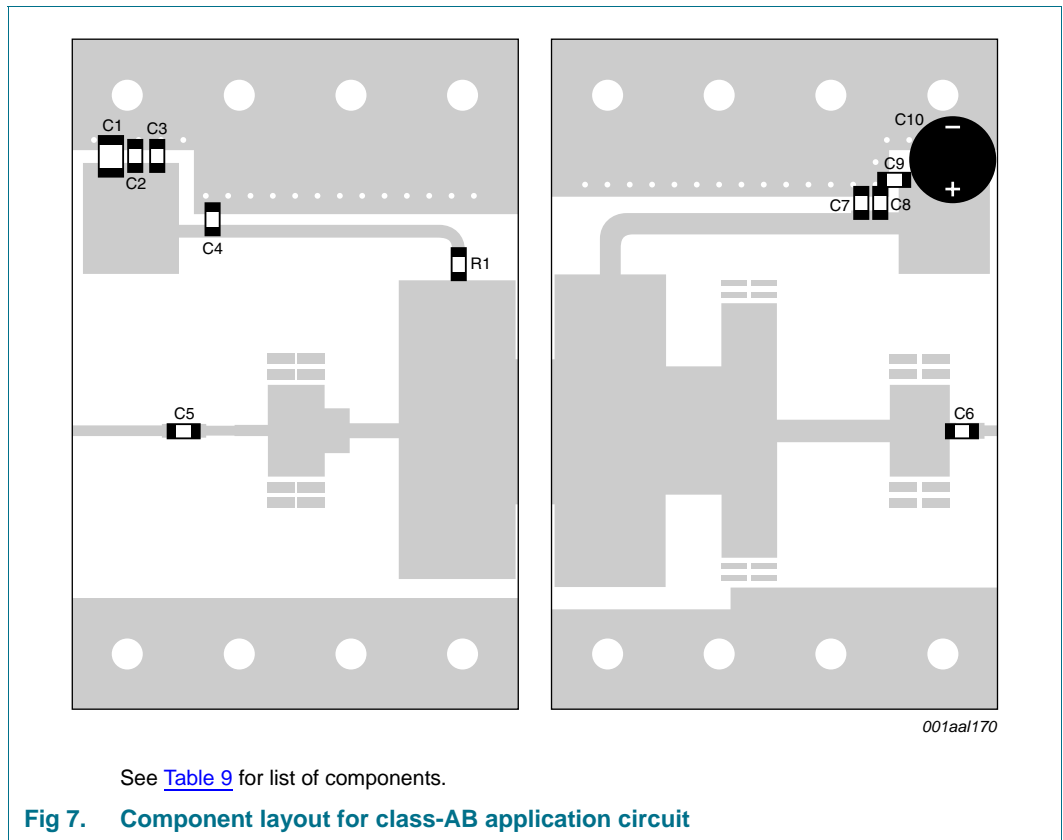


Table 9. List of components

See [Figure 7](#).

Striplines are on a Rogers Duroid 6006 Printed-Circuit Board (PCB); $\epsilon_r = 6.15$ F/m; thickness = 0.64 mm.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	10 μ F; 35 V	[1]
C2, C4	multilayer ceramic chip capacitor	51 pF	[2]
C3, C8	multilayer ceramic chip capacitor	1 nF	[2]
C5	multilayer ceramic chip capacitor	82 pF	[3]
C6, C7	multilayer ceramic chip capacitor	56 pF	[3]
C9	multilayer ceramic chip capacitor	100 pF	[3]
C10	electrolytic capacitor	47 μ F; 63 V	
R1	SMD resistor	10 Ω	0603

[1] American Technical Ceramics type 100A or capacitor of same quality.

[2] American Technical Ceramics type 100B or capacitor of same quality.

[3] American Technical Ceramics type 800B or capacitor of same quality.

8. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT502A

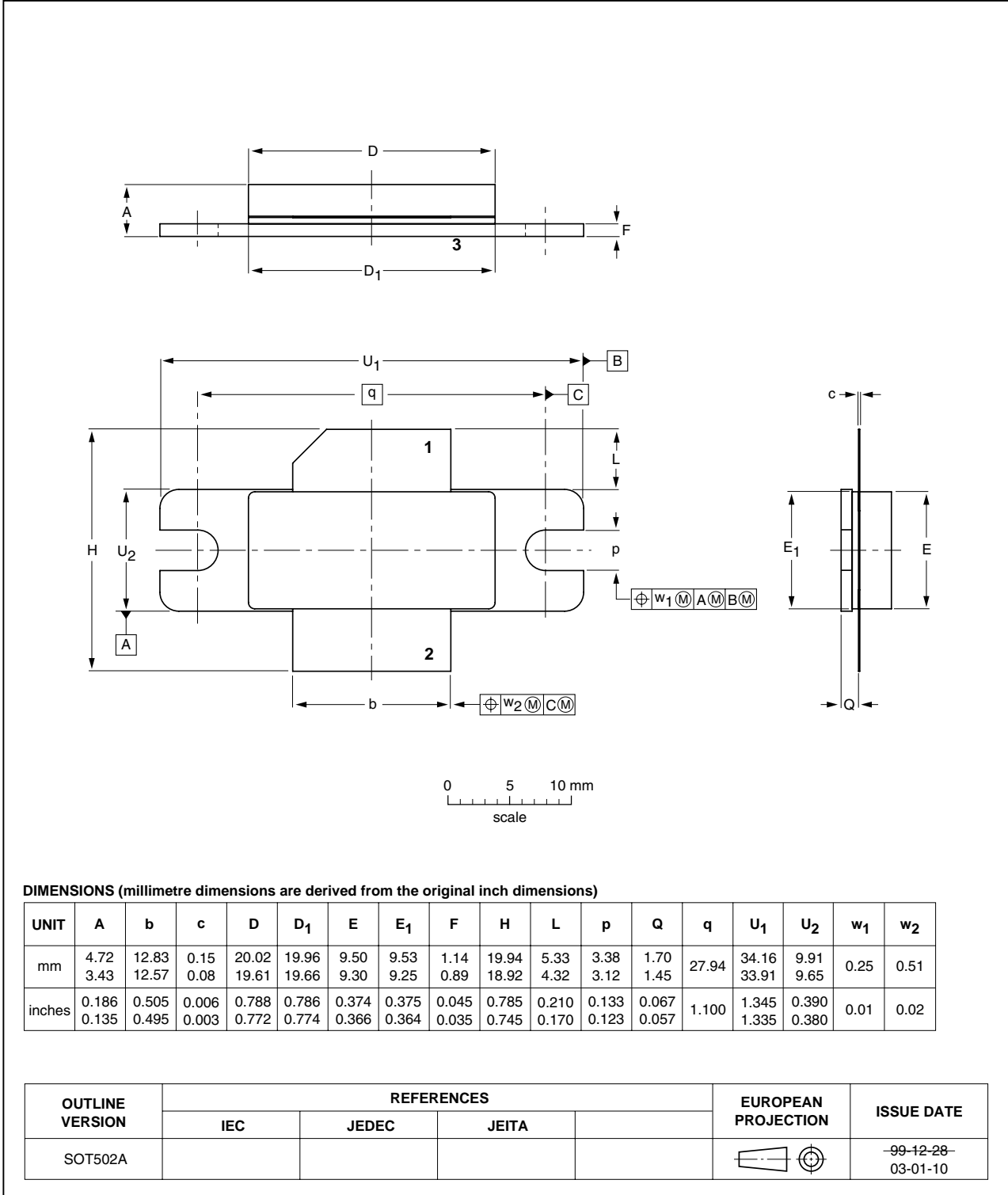


Fig 8. Package outline SOT502A

Earless flanged LDMOST ceramic package; 2 leads

SOT502B

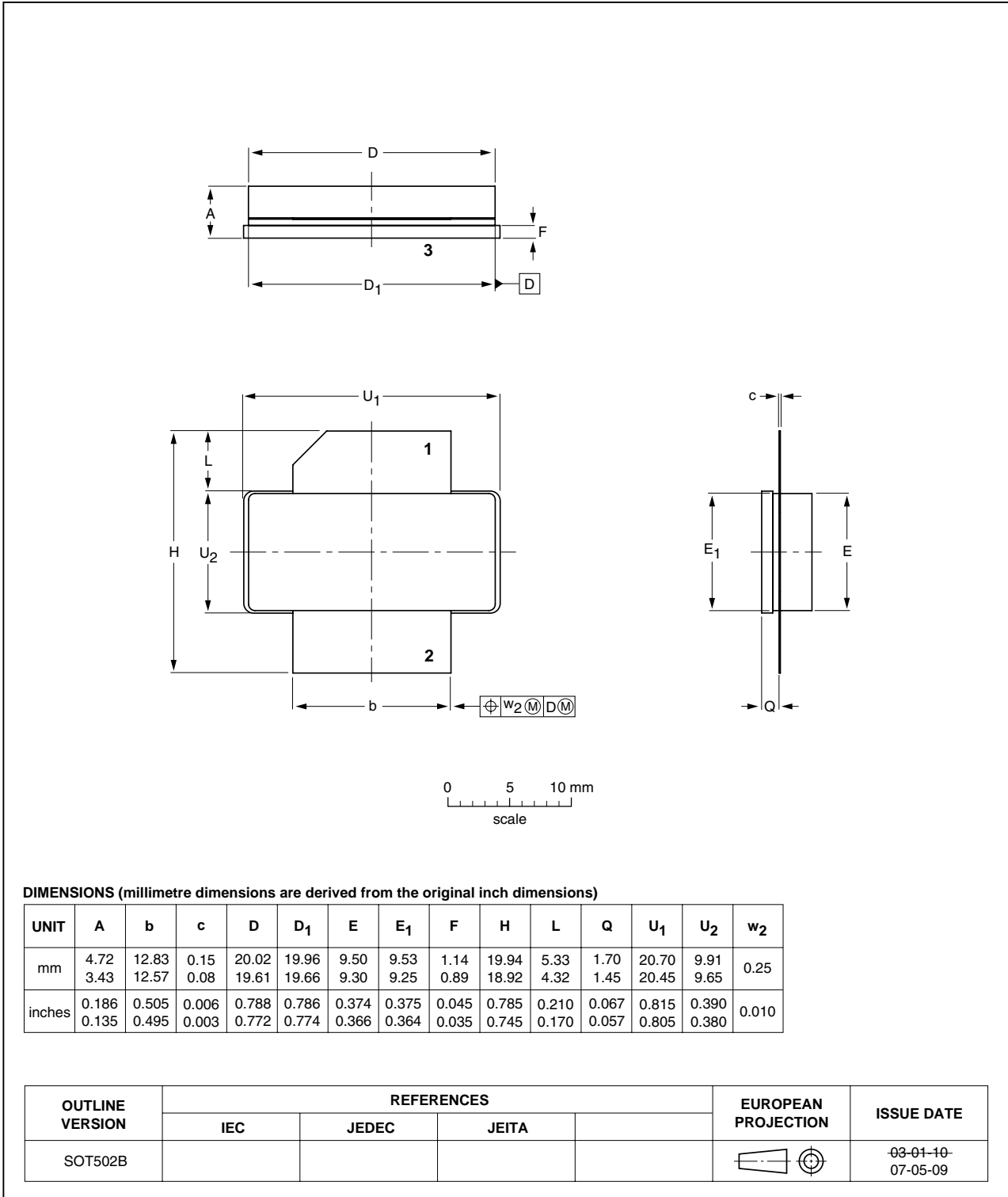


Fig 9. Package outline SOT502B

9. Abbreviations

Table 10. Abbreviations

Acronym	Description
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
RF	Radio Frequency
SMD	Surface Mounted Device
L-band	Long wave Band
VSWR	Voltage Standing-Wave Ratio

10. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLL6H1214L-250_1214LS-250_1	20091211	Objective data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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