MCP4021/2/3/4

Low-Cost NV Digital POT in SOT-23 with the WiperLock™ Technology

Features

- Nonvolatile Digital Potentiometer in SOT-23, MSOP and SOIC packages
- 64 Taps: 63 Resistors with Taps to V_{SS} and V_{DD}
- Simple Up/$\overline{\text{Down}}$ ($\text{U}/\overline{\text{D}}$) Protocol
- Automatic Recall of Saved Wiper Setting
- Resistance Values: 2.1 kΩ, 5 kΩ, 10 kΩ or 50 kΩ
- Low Tempco:
  - Absolute (Rheostat): 50 ppm (0°C to 70°C typ.)
  - Ratiometric (Potentiometer): 10 ppm (typ.)
- Low Wiper Resistance: 75Ω (typ.)
- WiperLock™ Technology to Secure the EEPROM
- High-Voltage Tolerant Digital Inputs: Up to 12V
- Low-Power Operation: 1 µA Max Static Current
- Wide Operating Voltage: 2.7V to 5.5V
- Extended Temperature Range: -40°C to +125°C

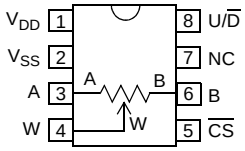
Applications

- Power Supply Trim and Calibration
- Mechanical Potentiometer Replacement in New Designs
- Instrumentation, Offset and Gain Adjust

Package Types

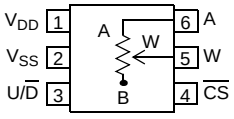
MCP4021

MSOP, SOIC
Potentiometer



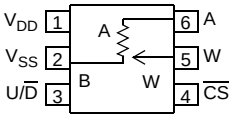
MCP4022

SOT-23-6
Rheostat



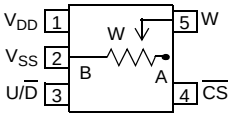
MCP4023

SOT-23-6
Potentiometer



MCP4024

SOT-23-5
Rheostat



Description

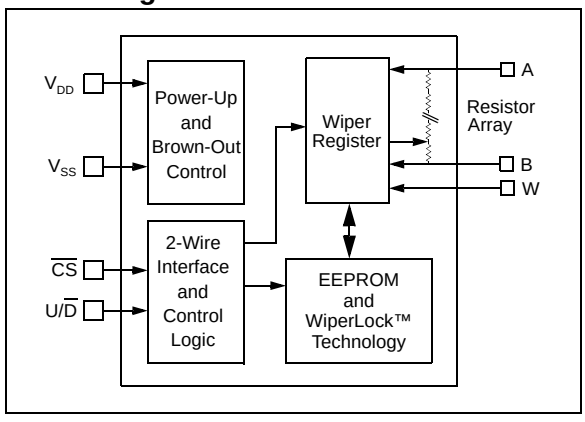
The MCP4021/2/3/4 devices are nonvolatile, 6-Bit digital potentiometers that are programmed through a simple Up/Down ($\text{U}/\overline{\text{D}}$) serial interface.

The MCP4021 device offers a voltage divider (potentiometer) with all terminals available on pins. The MCP4022 is a true rheostat, with both nodes of the variable resistor available on pins. The MCP4023 device offers a voltage divider (potentiometer) with one terminal connected to ground. The MCP4024 device is a Rheostat mode device with one terminal of the resistor connected to ground.

The simple $\text{U}/\overline{\text{D}}$ protocol uses the state of $\text{U}/\overline{\text{D}}$ at the falling edge of $\overline{\text{CS}}$ to determine if Increment or Decrement mode is desired. Subsequent rising edges of $\text{U}/\overline{\text{D}}$ move the wiper, which will not underflow 0h or overflow 3Fh. The new wiper setting can be saved to EEPROM, if desired, by selecting the state of $\text{U}/\overline{\text{D}}$ during the rising edge of $\overline{\text{CS}}$. The nonvolatile wiper enables the MCP4021/2/3/4 to operate with or without a microcontroller.

The MCP4021/2/3/4 device's WiperLock technology allows application-specific calibration settings to be secured in the EEPROM without requiring the use of an additional write-protect pin. This feature is enabled/disabled using commands where $\overline{\text{CS}} > V_{DD}$. Both $\overline{\text{CS}}$ and $\text{U}/\overline{\text{D}}$ inputs are tolerant of signals up to 12V. This allows the flexibility to multiplex the digital pot's control signals onto application signals for manufacturing/calibration.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DD} 6.5V

$\overline{CS}$ and U/$\overline{D}$ inputs w.r.t ..... V_{SS} -0.3V to 12.5V

A,B, and W terminals w.r.t ..... V_{SS} -0.3V to V_{DD} + 0.3V

Current at Input Pins .....±10 mA

Current at Supply Pins .....±10 mA

Current at Potentiometer Pins .....±2.5 mA

Storage temperature .....-65°C to +150°C

Ambient temp. with power applied .....-55°C to +125°C

ESD protection on all pins .....≥ 4 kV (HBM), ≥ 400V (MM)

Maximum Junction Temperature (T_J) .....+150°C

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

5V AC/DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply across the specified operating ranges. V_{DD} = +5.5V, T_A = -40°C to +125°C, 2 kΩ, 5 kΩ, 10 kΩ and 50 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, V_{SS} = 0V, T_A = +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Nominal Resistance	R_{AB}	—	2.1	—	kΩ	-202 devices **(Note 1)**
		—	5	—	kΩ	-502 devices **(Note 1)**
		—	10	—	kΩ	-103 devices **(Note 1)**
		—	50	—	kΩ	-503 devices **(Note 1)**
Nominal Resistance Tolerance	R/R_{AB}	—	—	20	%	
Nominal Resistance Tempco	$\Delta R/\Delta T$	—	50	—	ppm/°C	T_A = -20°C to 70°C
		—	100	—	ppm/°C	T_A = -40°C to 85°C
		—	150	—	ppm/°C	T_A = -40°C to 125°C
Ratiometeric Tempco	$\Delta V_{WA}/\Delta T$	—	10	—	ppm/°C	**MCP4021** and **MCP4023** only, code = 1Fh
Resolution	N		64		Taps	No Missing Codes
Potentiometer Integral Nonlinearity	INL	-1/2	±1/4	+1/2	LSb	**MCP4021/23** only **(Note 2)**
Potentiometer Differential Nonlinearity	DNL	-1/2	±1/4	+1/2	LSb	**MCP4021/23** only **(Note 2)**
Rheostat Integral Nonlinearity	R-INL	-1/2	±1/4	+1/2	LSb	**MCP4022/24** only
Rheostat Differential Nonlinearity	R-DNL	-1/2	±1/4	+1/2	LSb	**MCP4022/24** only
Wiper Resistance	R_W	—	75	125	Ω	**Note 3**
Full-scale Error	V_{WFSE}	-0.5	-0.1	+0.5	LSb	Code 3Fh **(Note 6)**
Zero-scale Error	V_{WZSE}	-0.5	+0.1	+0.5	LSb	Code 00h **(Note 7)**
Resistor Terminal Voltage Range	V_A, V_W, V_B	Vss	—	V_{DD}	V	**Note 4**

Note 1: Nominal resistance is defined as resistance from terminal A to terminal B. Note that R_W would be added to R_{AB} on rheostat devices for measured end-to-end resistance.

2: INL and DNL are measured at V_W with $V_A = V_{DD}$ and $V_B = V_{SS}$.

3: **MCP4021/23** only, test conditions are: I_W = 1.9 mA, code = 00h,
2 kΩ **MCP4022/24** only, test conditions are (**MCP4022** includes V_{WZSE}, while **MCP4024** includes V_{WFSE}): 2.25 mA.
5 kΩ **MCP4022/24** only, test conditions are (**MCP4022** includes V_{WZSE}, while **MCP4024** includes V_{WFSE}): 1.4 mA.
10 kΩ **MCP4022/24** only, test conditions are (**MCP4022** includes V_{WZSE}, while **MCP4024** includes V_{WFSE}): 450 µA.
50 kΩ **MCP4022/24** only, test conditions are (**MCP4022** includes V_{WZSE}, while **MCP4024** includes V_{WFSE}): 90µA.

4: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

5: This parameter is not tested.

6: **MCP4024** only – includes V_{WZSE}, code 00h.

7: **MCP4022** only – includes V_{WFSE}, code 3Fh.

5V AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply across the specified operating ranges. V_{DD} = +5.5V, T_A = -40°C to +125°C, 2 kΩ, 5 kΩ, 10 kΩ and 50 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, V_{SS} = 0V, T_A = +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Maximum current through A, W or B	I_W	—	2.5	—	mA	**Note 5**
Leakage current into A, W or B	I_{WL}	—	100	—	nA	**MCP4021** A = W = B = V_{SS} **MCP4022** A = W **MCP4023** A = W = V_{SS} **MCP4024** W = V_{SS}
Capacitance (P_A)	C_{AW}	—	75	—	pF	f =1 MHz, code = 1Fh
Capacitance (P_w)	C_W	—	120	—	pF	f =1 MHz, code = 1Fh
Capacitance (P_B)	C_{BW}	—	75	—	pF	f =1 MHz, code = 1Fh
Bandwidth -3 dB	BW	—	1	—	MHz	Code = 1F, output load = 30 pF
Digital Inputs/Outputs ($\overline{CS}$, U/$\overline{D}$)						
High-Input Threshold	V_{IH}	0.7 V_{DD}	—	—	V	
Low-Input Threshold	V_{IL}	—	—	0.3 V_{DD}	V	
$\overline{CS}$ High-Voltage Input Threshold	V_{PP}	—	7.8	—	V	Threshold for WiperLock™ Technology
$\overline{CS}$ and U/$\overline{D}$ High-Voltage Limit	V_{MAX}	—	12.5	—	V	Pin can tolerate V_{MAX} or less. **Note 5**
$\overline{CS}$ Pull-up/Pull-down Resistance	R_{CS}	—	16	—	kΩ	V_{DD} = 5.5V, $V_{\overline{CS}}$ = 3V **(Note 5)**
$\overline{CS}$ Weak Pull-up/Pull-down Current	I_{PU}	—	170	—	µA	V_{DD} = 5.5V, $V_{\overline{CS}}$ = 3V **(Note 5)**
Input Leakage Current	I_{IL}	-1	—	1	µA	V_{IN} = V_{DD}
Pin Capacitance	C_{IN}, C_{OUT}	—	10	—	pF	f_c = 1 MHz
EEPROM						
Endurance	$E_{ndurance}$	—	1M	—	Cycles	
EEPROM Range	N	0h	—	3Fh	hex	
Initial Factory Setting	N		1Fh		hex	WiperLock Technology = Off
Power Requirements						
Operating Voltage Range	V_{DD}	2.7	—	5.5	V	
Supply Current, Active	I_{DD}	—	45	—	µA	$\overline{CS}$ = V_{SS}, $f_{U/\overline{D}}$ = 1 MHz
Supply Current, Static	I_{SHDN}	—	0.3	1	µA	
Supply Current, EE Write	I_{WRITE}	—	0.6	3	mA	T_A = +25°C
Power Supply Sensitivity	PSS	—	0.0015	0.0035	%/%	**MCP4021** & **MCP4023** only V_{DD} = 4.5V – 5.5V, V_A = 4.5V Code = 1Fh

Note 1: Nominal resistance is defined as resistance from terminal A to terminal B. Note that R_W would be added to R_{AB} on rheostat devices for measured end-to-end resistance.

2: INL and DNL are measured at V_W with V_A = V_{DD} and V_B = V_{SS}.

3: **MCP4021/23** only, test conditions are: I_W = 1.9 mA, code = 00h,
2 kΩ **MCP4022/24** only, test conditions are (**MCP4022** includes V_{WZSE}, while **MCP4024** includes V_{WFSE}): 2.25 mA.
5 kΩ **MCP4022/24** only, test conditions are (**MCP4022** includes V_{WZSE}, while **MCP4024** includes V_{WFSE}): 1.4 mA.
10 kΩ **MCP4022/24** only, test conditions are (**MCP4022** includes V_{WZSE}, while **MCP4024** includes V_{WFSE}): 450 µA.
50 kΩ **MCP4022/24** only, test conditions are (**MCP4022** includes V_{WZSE}, while **MCP4024** includes V_{WFSE}): 90µA.

4: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

5: This parameter is not tested.

6: **MCP4024** only – includes V_{WZSE}, code 00h.

7: **MCP4022** only – includes V_{WFSE}, code 3Fh.

2.7V AC/DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply across the specified operating ranges. V_{DD} = +2.7V, T_A = -40°C to +125°C, 2 kΩ, 5 kΩ, 10 kΩ and 50 kΩ devices. Typical specifications represent values for V_{DD} = 2.7V, V_{SS} = 0V, T_A = +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Nominal Resistance	R_{AB}	—	2.1	—	kΩ	-202 devices **(Note 1)**
		—	5	—	kΩ	-502 devices **(Note 1)**
		—	10	—	kΩ	-103 devices **(Note 1)**
		—	50	—	kΩ	-503 devices **(Note 1)**
Nominal Resistance Tolerance	R/R_{AB}	—	—	20	%	
Nominal Resistance Tempco	$\Delta R/\Delta T$	—	50	—	ppm/°C	T_A = -20°C to 70°C
		—	100	—	ppm/°C	T_A = -40°C to 85°C
		—	150	—	ppm/°C	T_A = -40°C to 125°C
Ratiometeric Tempco	$\Delta V_{WA}/\Delta T$	—	10	—	ppm/°C	**MCP4021** and **MCP4023** only, code = 1Fh
Resolution	N		64		Taps	No Missing Codes
Potentiometer Integral Nonlinearity	INL	-1/2	±1/4	+1/2	LSb	**MCP4021/23** only **(Note 2)**
Potentiometer Differential Nonlinearity	DNL	-1/2	±1/4	+1/2	LSb	MCP4021/23 only **(Note 2)**
Rheostat Integral Nonlinearity	R-INL	-8.5	+4.5	+8.5	LSb	2 kΩ **MCP4022/24** only
		-5.5	+2.5	+5.5	LSb	5 kΩ **MCP4022/24** only
		-3	+1	+3	LSb	10 kΩ **MCP4022/24** only
		-1	+1/4	+1	LSb	50 kΩ **MCP4022/24** only
Rheostat Differential Nonlinearity	R-DNL	-1	+1/2	+2	LSb	2 kΩ **MCP4022/24** only
		-1	+1/4	+1.25	LSb	5 kΩ **MCP4022/24** only
		-1/2	0	+1/2	LSb	10 kΩ **MCP4022/24** only
		-1/2	0	+1/2	LSb	50 kΩ **MCP4022/24** only
Wiper Resistance	R_W	—	75	125	Ω	**Note 3**
Full-scale Error	V_{WFSE}	-0.5	-0.1	+0.5	LSb	Code 3Fh **(Note 6)**
Zero-scale Error	V_{WZSE}	-0.5	+0.1	+0.5	LSb	Code 00h **(Note 7)**
Resistor Terminal Voltage Range	$V_{A,W}$	Vss	—	V_{DD}	V	**Note 4**
Maximum current into A or W	I_W	—	2.5	—	mA	**Note 5**
Leakage current into A or W	I_{WL}	—	100	—	nA	**MCP4021** A = W = B = V_{SS} **MCP4022** A = W **MCP4023** A = W = V_{SS} **MCP4024** W = V_{SS}
Capacitance (P_A)	C_{AW}	—	75	—	pF	f =1 MHz, Code = 1Fh
Capacitance (P_w)	C_W	—	120	—	pF	f =1 MHz, Code = 1Fh
Capacitance (P_B)	C_{BW}	—	75	—	pF	f =1 MHz, Code = 1Fh
Bandwidth -3dB	BW	—	1	—	MHz	Code = 1F, Output Load = 30 pF

Note 1: Nominal Resistance is defined as resistance from terminal A to terminal B. Note that R_W would be added to R_{AB} on Rheostat devices for measured end-to-end resistance.

2: INL and DNL are measured at V_W with $V_A = V_{DD}$ and $V_B = V_{SS}$.

3: MCP4021/23 only, test conditions are: I_W = 1.9 mA, Code = 00h,
2 kΩ **MCP4022/24** only, test conditions are (**MCP4022** includes V_{WZSE}, while **MCP4024** includes V_{WFSE}): 1.1 mA.
5 kΩ **MCP4022/24** only, test conditions are (**MCP4022** includes V_{WZSE}, while **MCP4024** includes V_{WFSE}): 450 µA.
10 kΩ **MCP4022/24** only, test conditions are (**MCP4022** includes V_{WZSE}, while **MCP4024** includes V_{WFSE}): 210 µA.
50 kΩ **MCP4022/24** only, test conditions are (**MCP4022** includes V_{WZSE}, while **MCP4024** includes V_{WFSE}): 40 µA.

4: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

5: This parameter is not tested.

6: **MCP4024** only – includes V_{WZSE}, code 00h.

7: **MCP4022** only – includes V_{WFSE}, code 3Fh.

2.7V AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply across the specified operating ranges. V_{DD} = +2.7V, T_A = -40°C to +125°C, 2 kΩ, 5 kΩ, 10 kΩ and 50 kΩ devices. Typical specifications represent values for V_{DD} = 2.7V, V_{SS} = 0V, T_A = +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Digital Inputs/Outputs ($\overline{CS}$, U/$\overline{D}$)						
High-Input Threshold	V_{IH}	$0.7V_{DD}$	—	—	V	
Low-Input Threshold	V_{IL}	—	—	$0.3V_{DD}$	V	
Input Leakage Current	I_{IL}	-1	—	1	µA	$V_{IN} = V_{DD}$
$\overline{CS}$ High-Voltage Input Threshold	V_{PP}	—	7.8	—	V	Threshold for WiperLock Technology
$\overline{CS}$ and U/$\overline{D}$ High-Voltage Limit	V_{MAX}	—	12.5	—	V	Pin can tolerate V_{MAX} or less. **Note 5**
Pin Capacitance	C_{IN}, C_{OUT}	—	10	—	pF	f_c = 1 MHz
EEPROM						
Endurance	$E_{ndurance}$	—	1M	—	Cycles	
EEPROM Range	N	0h	—	3Fh	hex	
Initial Factory Setting	N		1Fh		hex	WiperLock Technology = Off
Power Requirements						
Operating Voltage Range	V_{DD}	2.7	—	5.5	V	
Supply Current, Active	I_{DD}	—	15	—	µA	$\overline{CS}$ = V_{SS}, $f_{U/\overline{D}}$ = 1 MHz
Supply Current, Static	I_{SHDN}	—	0.3	1	µA	
Supply Current, EE Write	I_{WRITE}	—	0.6	3	mA	T_A = +25°C
Power Supply Sensitivity	PSS	—	0.0015	0.0035	%/%	**MCP4021** and **MCP4023** only V_{DD} = 2.7V – 4.5V, V_A = 2.7V, Code = 1Fh

Note 1: Nominal Resistance is defined as resistance from terminal A to terminal B. Note that R_W would be added to R_{AB} on Rheostat devices for measured end-to-end resistance.

2: INL and DNL are measured at V_W with $V_A = V_{DD}$ and $V_B = V_{SS}$.

3: MCP4021/23 only, test conditions are: I_W = 1.9 mA, Code = 00h,
2 kΩ **MCP4022/24** only, test conditions are (**MCP4022** includes V_{WZSE}, while **MCP4024** includes V_{WFSE}): 1.1 mA.
5 kΩ **MCP4022/24** only, test conditions are (**MCP4022** includes V_{WZSE}, while **MCP4024** includes V_{WFSE}): 450 µA.
10 kΩ **MCP4022/24** only, test conditions are (**MCP4022** includes V_{WZSE}, while **MCP4024** includes V_{WFSE}): 210 µA.
50 kΩ **MCP4022/24** only, test conditions are (**MCP4022** includes V_{WZSE}, while **MCP4024** includes V_{WFSE}): 40 µA.

4: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

5: This parameter is not tested.

6: **MCP4024** only – includes V_{WZSE}, code 00h.

7: **MCP4022** only – includes V_{WFSE}, code 3Fh.

SERIAL TIMING CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply across the specified operating ranges. Extended (E): V_{DD} = +2.7V to 5.5V, T_A = -40°C to +125°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{CS}$ Low Time	t_{CSLO}	5	—	—	µs	
$\overline{CS}$ High Time	t_{CSHI}	500	—	—	ns	
LV U/$\overline{D}$ to $\overline{CS}$ Hold Time	t_{LUC}	500	—	—	ns	
LV $\overline{CS}$ to U/$\overline{D}$ Low Setup Time	t_{LCUF}	500	—	—	ns	
LV $\overline{CS}$ to U/$\overline{D}$ High Setup Time	t_{LCUR}	3	—	—	µs	
U/$\overline{D}$ High Time	t_{HI}	500	—	—	ns	
U/$\overline{D}$ Low Time	t_{LO}	500	—	—	ns	
Up / $\overline{Down}$ Toggle Frequency	f_{UD}	—	—	1	MHz	
HV U/$\overline{D}$ to $\overline{CS}$ Hold Time	t_{HUC}	1.5	—	—	µs	
HV $\overline{CS}$ to U/$\overline{D}$ Low Setup Time	t_{HCUF}	8	—	—	µs	
HV $\overline{CS}$ to U/$\overline{D}$ High Setup Time	t_{HCUR}	4.5	—	—	µs	
Wiper Settling Time	t_S	0.5	—	—	µs	2 kΩ, C_L=100pF
		1	—	—	µs	5 kΩ, C_L=100pF
		2	—	—	µs	10 kΩ, C_L=100pF
		10	5	—	µs	50 kΩ, C_L=100pF
Wiper Response on Power-up	t_{PU}	—	200	—	ns	
Internal EEPROM write time	twc	—	—	5	ms	

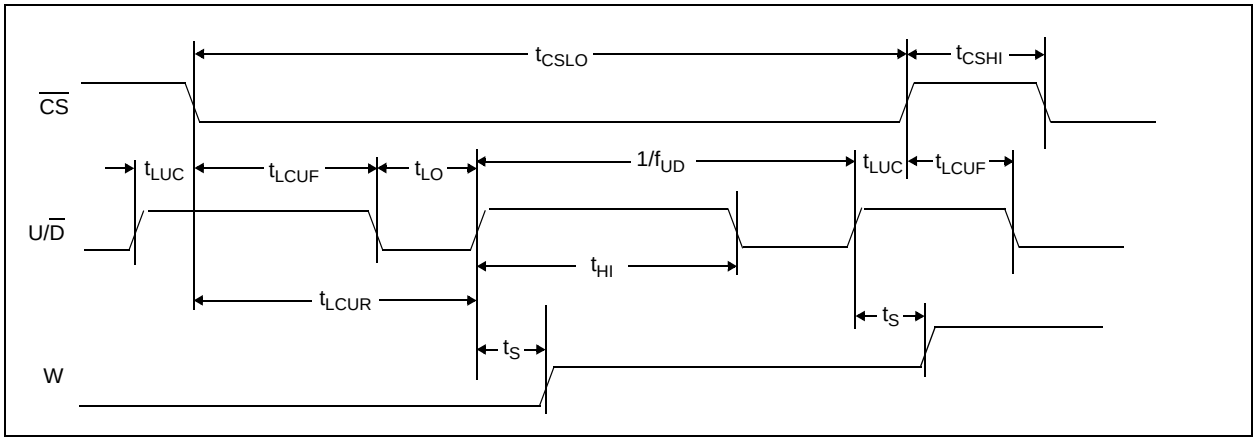


FIGURE 1-1: *Low-Voltage Increment Timing.*

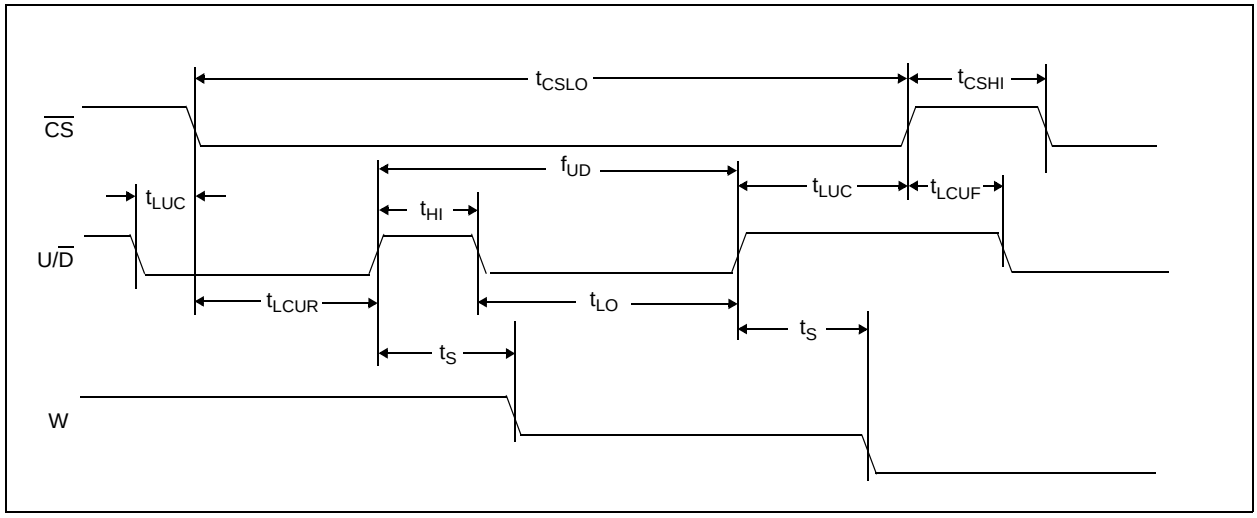


FIGURE 1-2: *Low-Voltage Decrement Timing.*

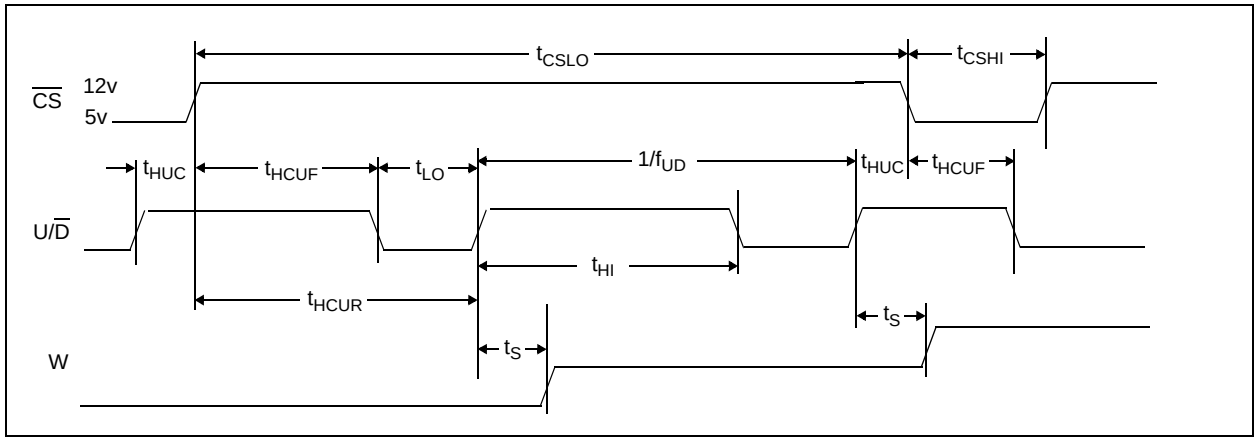


FIGURE 1-3: *High-Voltage Increment Timing.*

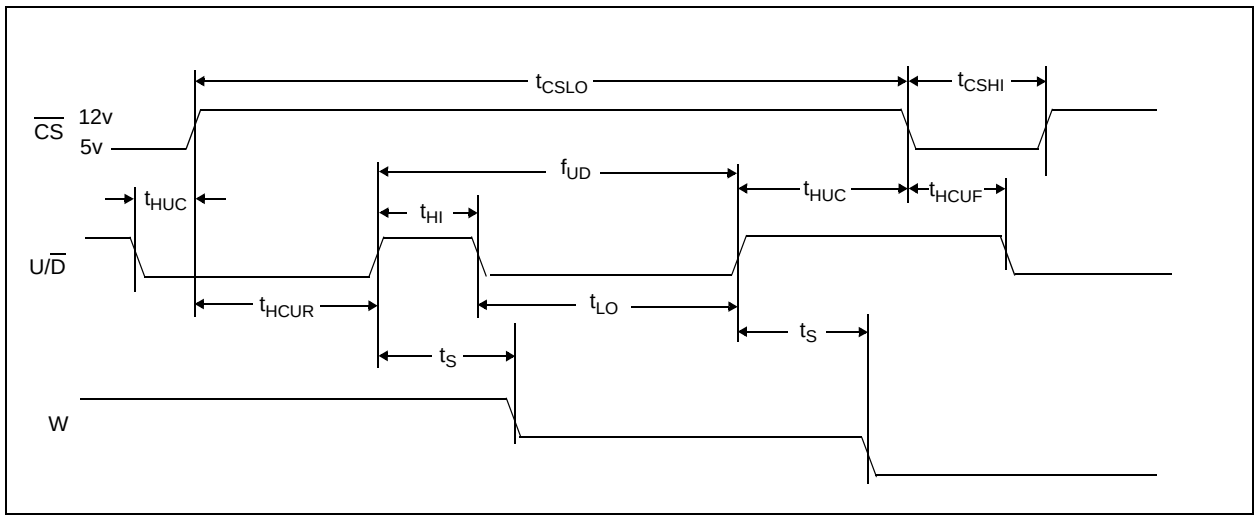


FIGURE 1-4: *High-Voltage Decrement Timing.*

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, AV_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 6L-SOT-23	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	

Note 1: The MCP4021/2/3/4 family of DACs operate over this extended temperature range, but with reduced performance. Operation in this range must not cause T_J to exceed the Maximum Junction Temperature of 150°C.

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

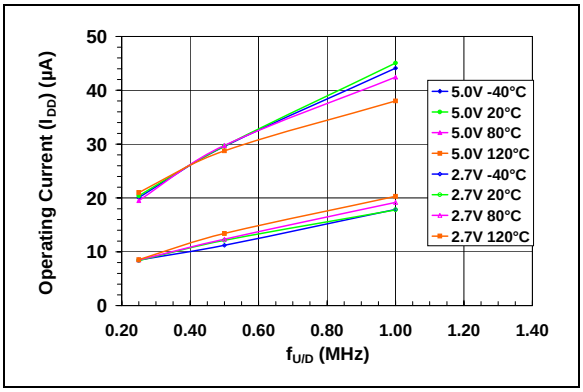


FIGURE 2-1: *Active Current (I_{DD}) vs. U/$\overline{D}$ Frequency ($f_{U/\overline{D}}$) and Ambient Temperature (V_{DD} = 2.7V and 5.5V).*

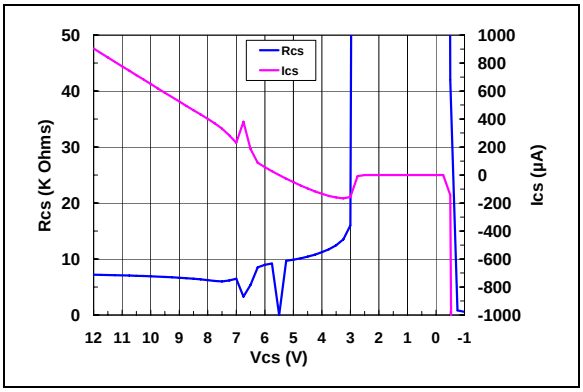


FIGURE 2-4: *$\overline{CS}$ Pull-up/Pull-down Resistance ($R_{\overline{CS}}$) and Current ($I_{\overline{CS}}$) vs. $\overline{CS}$ Input Voltage ($V_{\overline{CS}}$) (V_{DD} = 5.5V).*

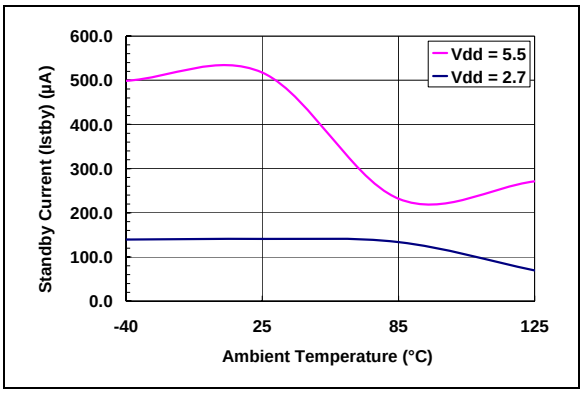


FIGURE 2-2: *Write Current (I_{WRITE}) vs. Ambient Temperature and V_{DD}.*

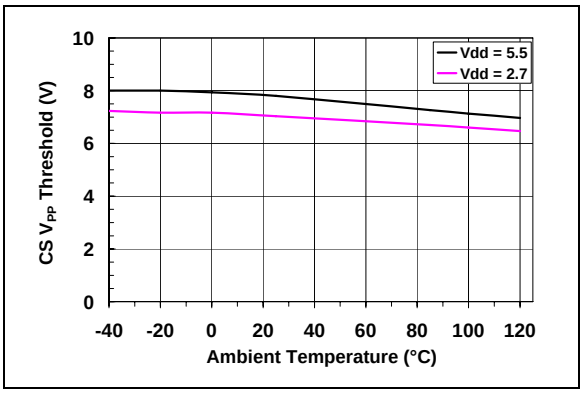


FIGURE 2-5: *$\overline{CS}$ High Input Threshold vs. Ambient Temperature and V_{DD}.*

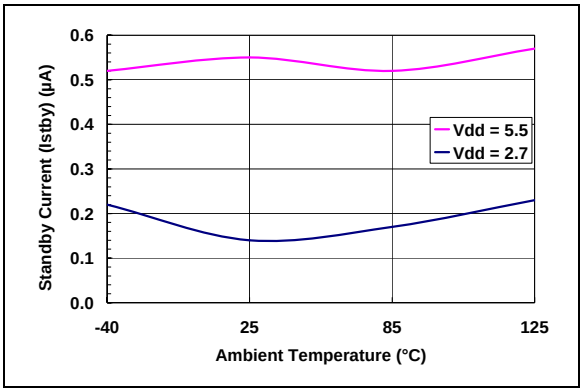


FIGURE 2-3: *Standby Current (I_{SHDN}) vs. Ambient Temperature and V_{DD}. ($\overline{CS}$ = V_{DD}).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

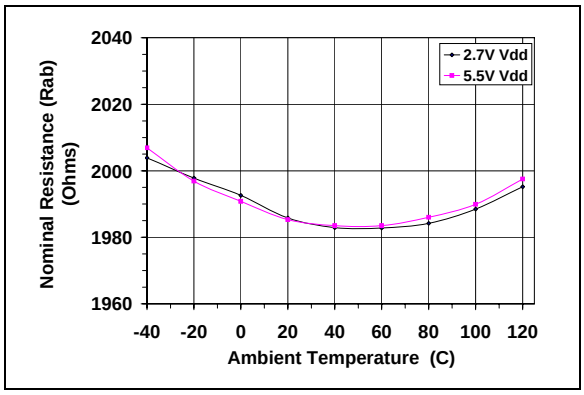


FIGURE 2-6: *2 kΩ – Nominal Resistance (Ω) vs. Ambient Temperature and V_{DD}.*

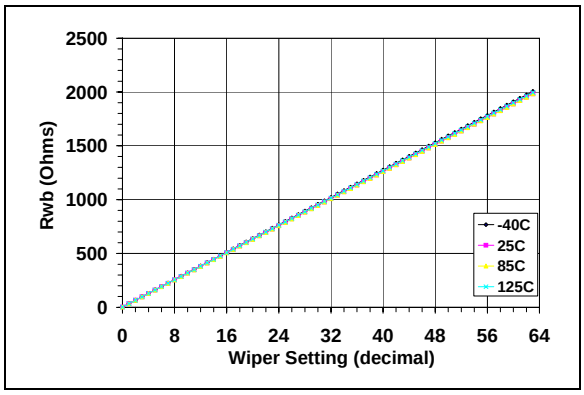


FIGURE 2-9: *2 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature.*

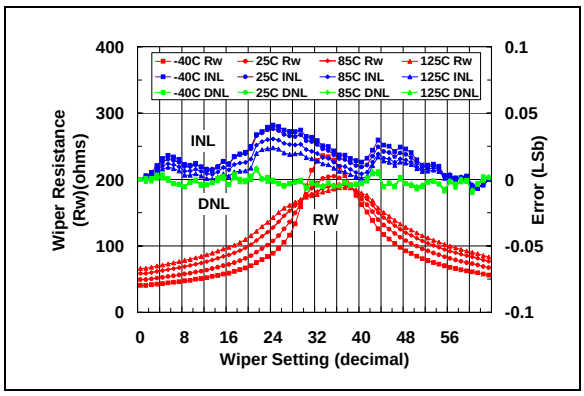


FIGURE 2-7: *2 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 2.7V).*

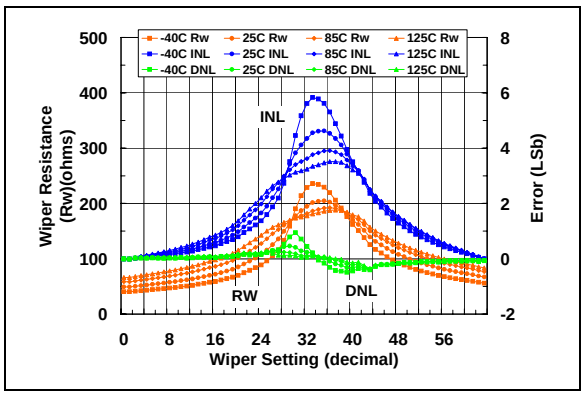


FIGURE 2-10: *2 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 2.7V).*

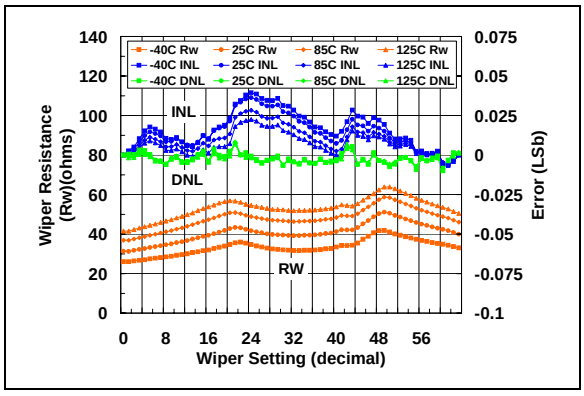


FIGURE 2-8: *2 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

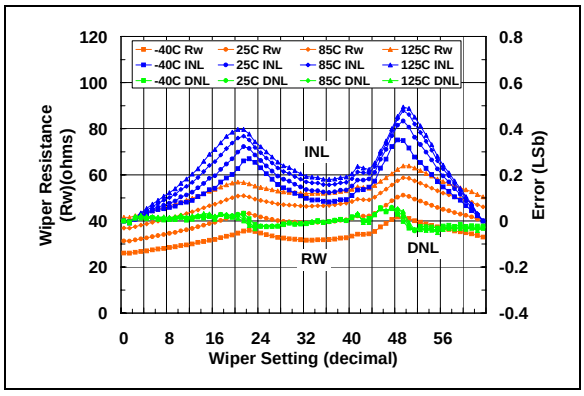


FIGURE 2-11: *2 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

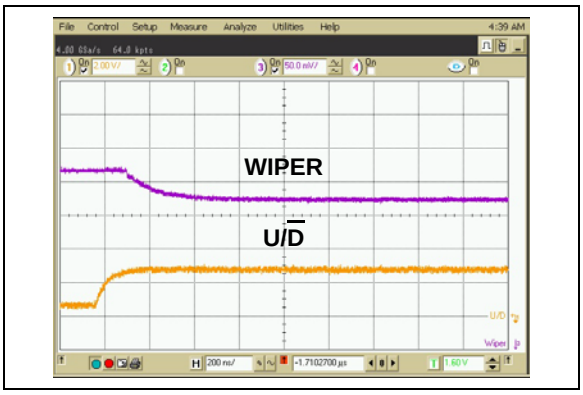


FIGURE 2-12: *2 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD}=2.7V).*

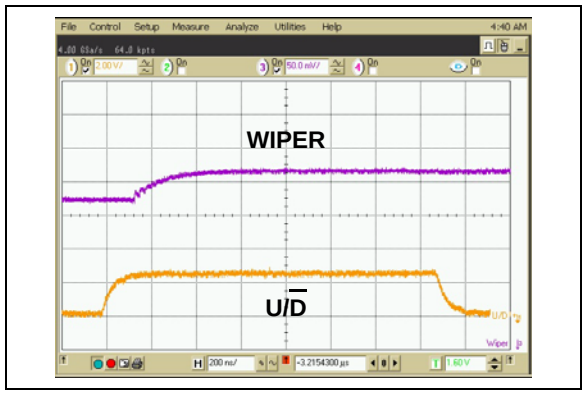


FIGURE 2-15: *2 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD}=2.7V).*

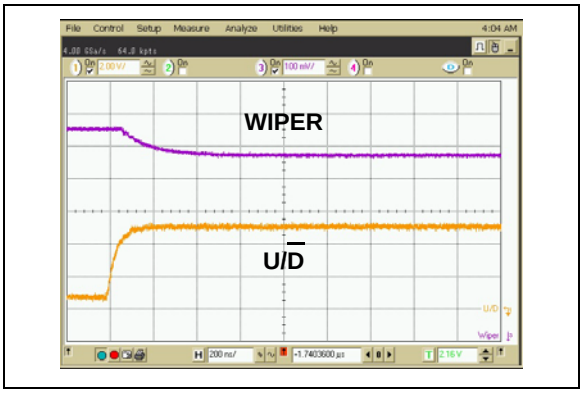


FIGURE 2-13: *2 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD}=5.5V).*

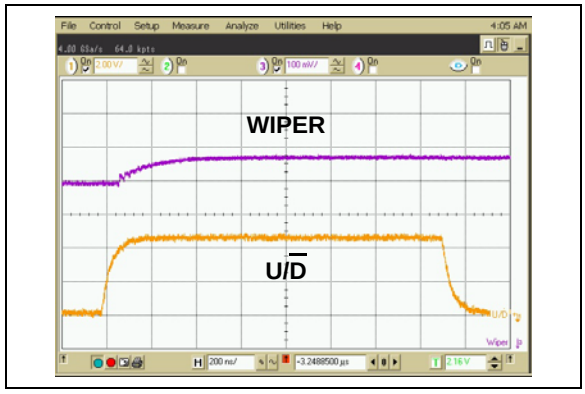


FIGURE 2-16: *2 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD}=5.5V).*

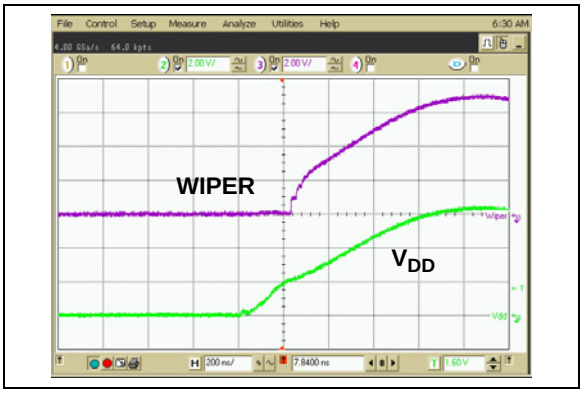


FIGURE 2-14: *2 kΩ – Power-Up Wiper Response Time.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

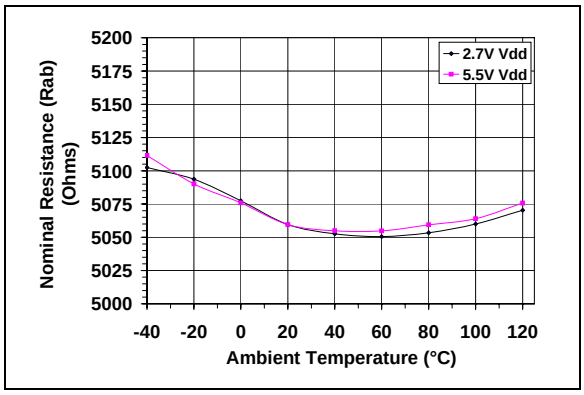


FIGURE 2-17: *5 kΩ – Nominal Resistance (Ω) vs. Ambient Temperature and V_{DD}.*

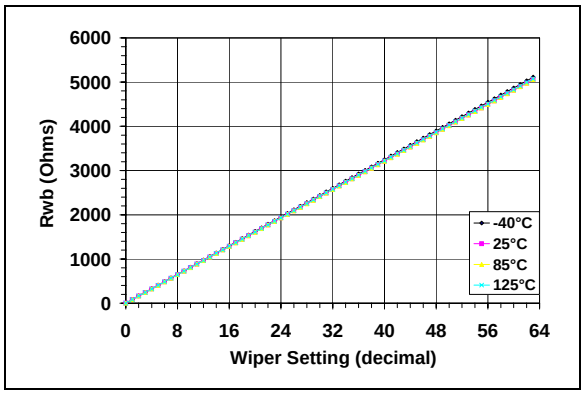


FIGURE 2-20: *5 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature.*

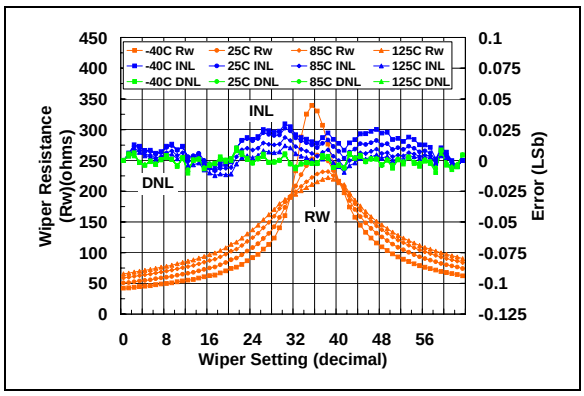


FIGURE 2-18: *5 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 2.7V).*

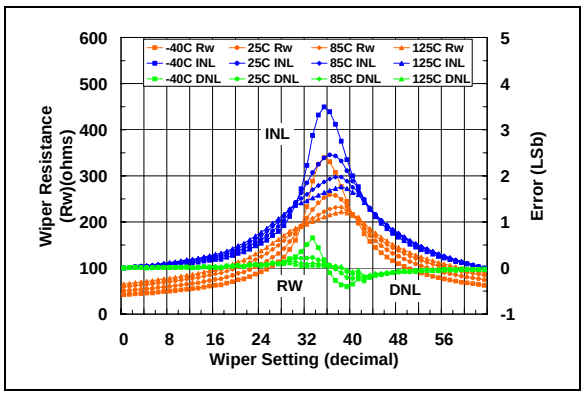


FIGURE 2-21: *5 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 2.7V).*

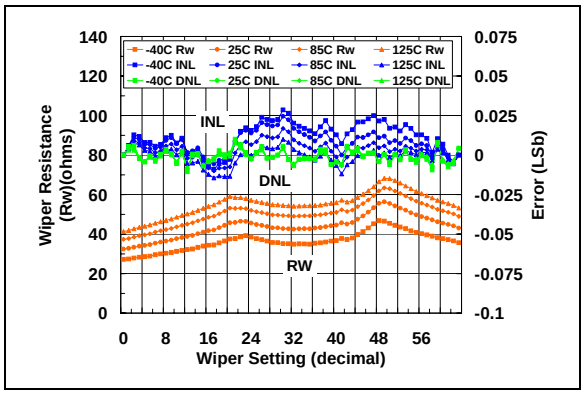


FIGURE 2-19: *5 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

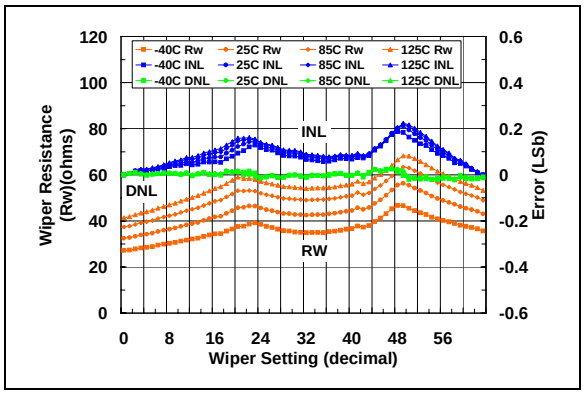


FIGURE 2-22: *5 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

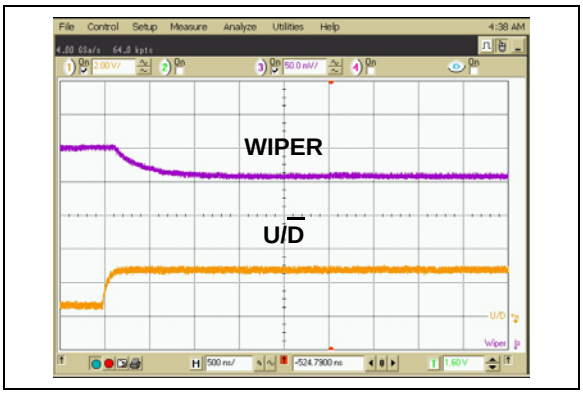


FIGURE 2-23: *5 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD}=2.7V).*

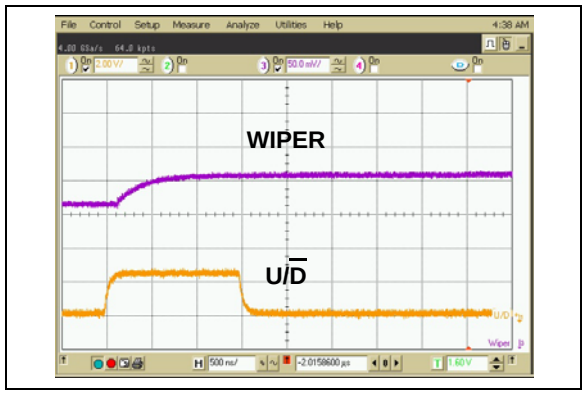


FIGURE 2-25: *5 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD}=2.7V).*

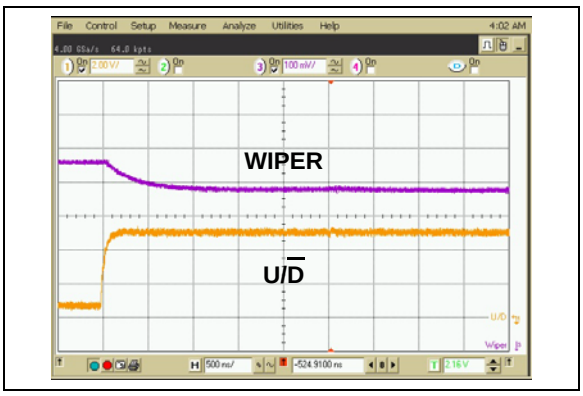


FIGURE 2-24: *5 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD}=5.5V).*

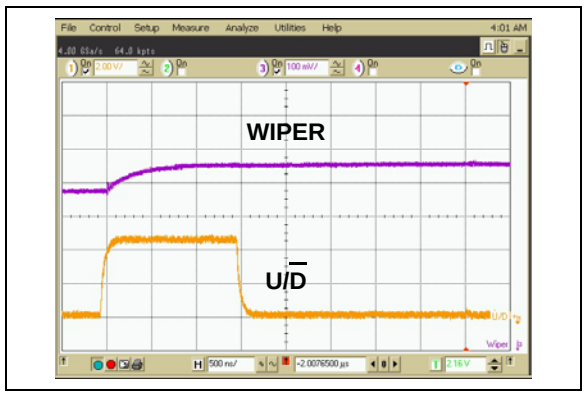


FIGURE 2-26: *5 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD}=5.5V).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

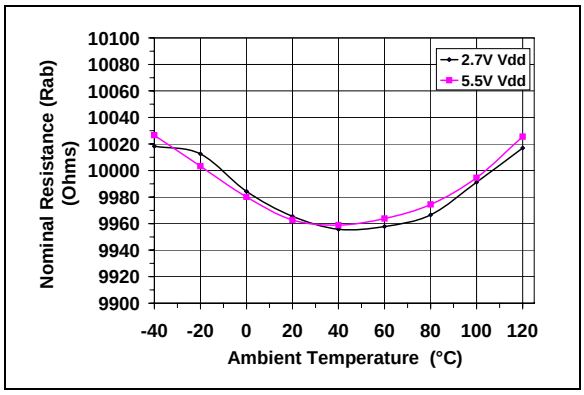


FIGURE 2-27: *10 kΩ – Nominal Resistance (Ω) vs. Ambient Temperature and V_{DD}.*

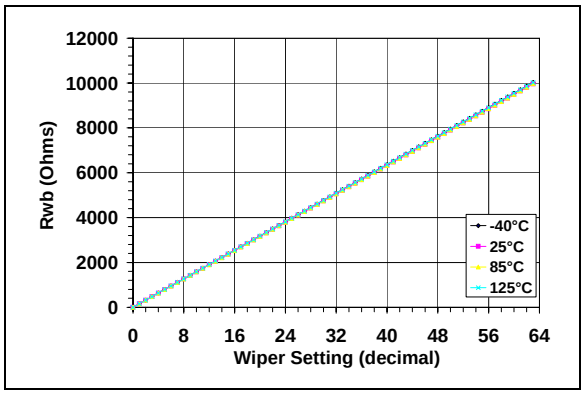


FIGURE 2-30: *10 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature.*

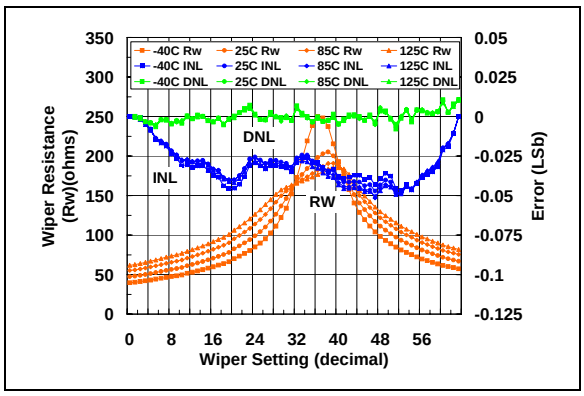


FIGURE 2-28: *10 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 2.7V).*

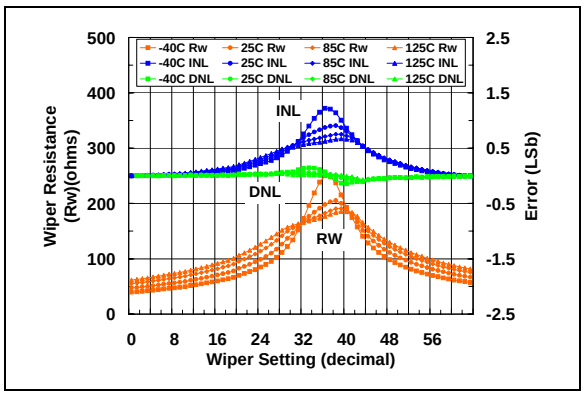


FIGURE 2-31: *10 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 2.7V).*

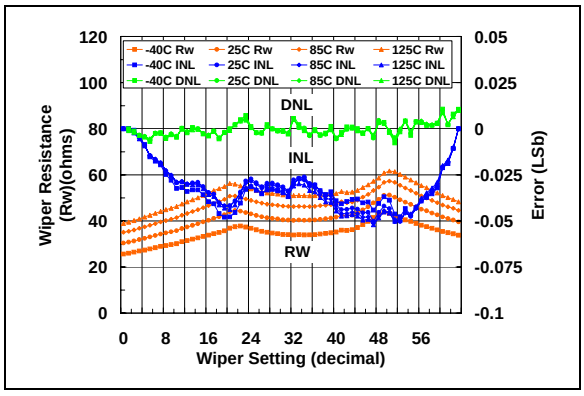


FIGURE 2-29: *10 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

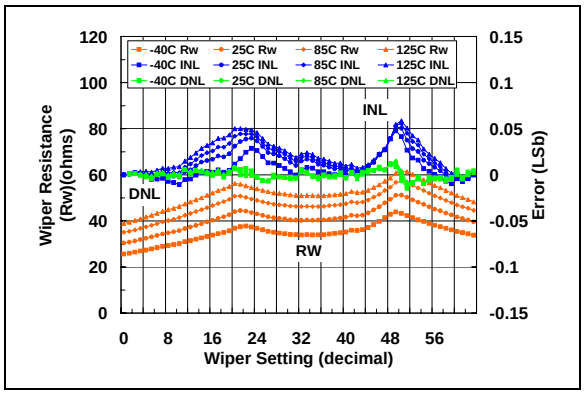


FIGURE 2-32: *10 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

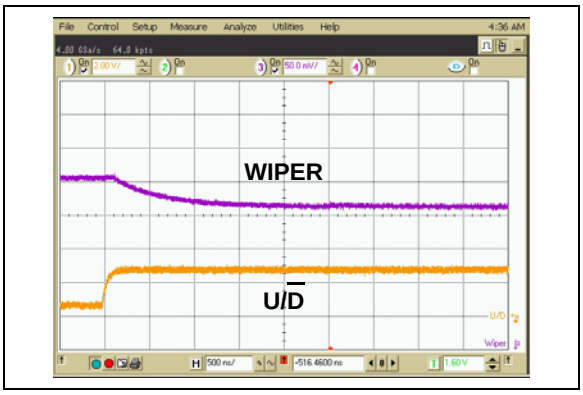


FIGURE 2-33: *10 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD}=2.7V).*

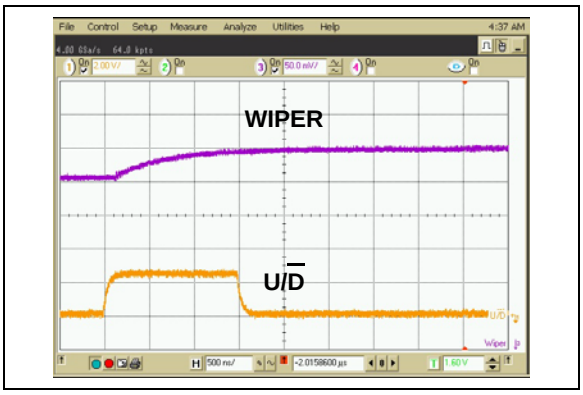


FIGURE 2-35: *10 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD}=2.7V).*

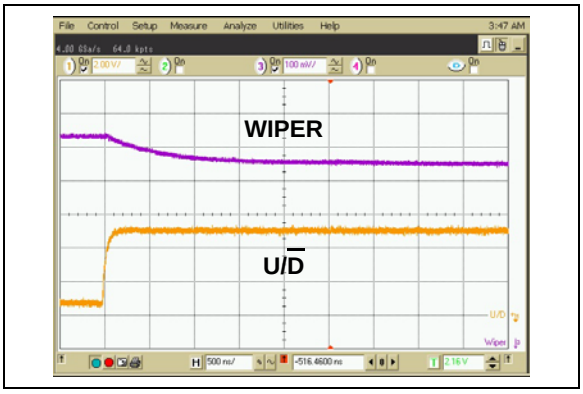


FIGURE 2-34: *10 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD}=5.5V).*

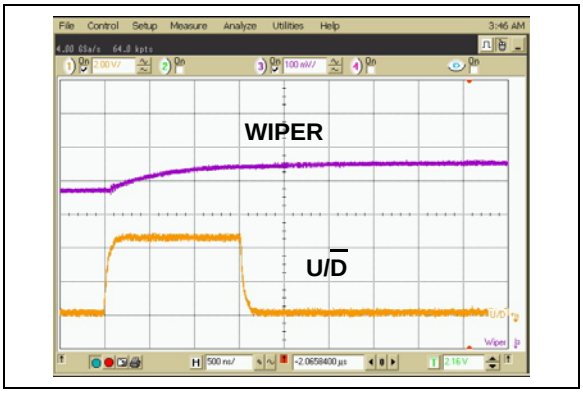


FIGURE 2-36: *10 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD}=5.5V).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

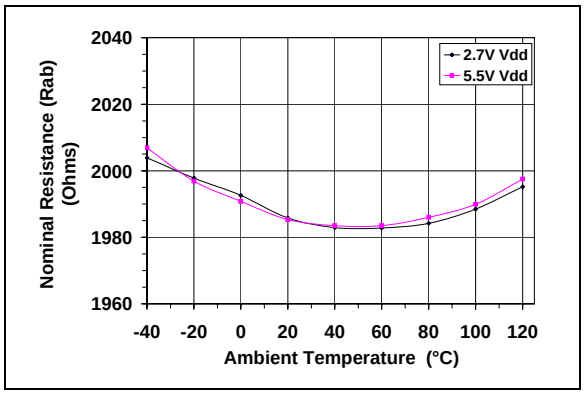


FIGURE 2-37: *50 kΩ – Nominal Resistance (Ω) vs. Ambient Temperature and V_{DD}.*

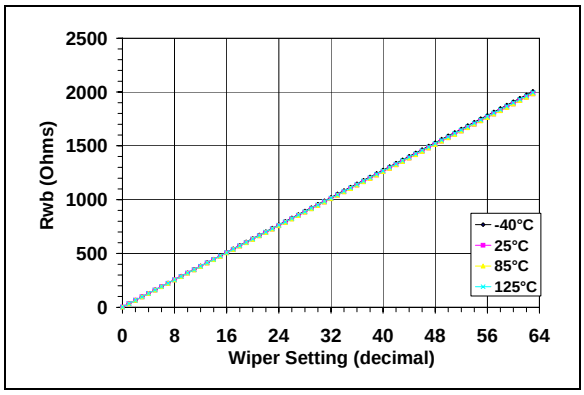


FIGURE 2-40: *50 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature.*

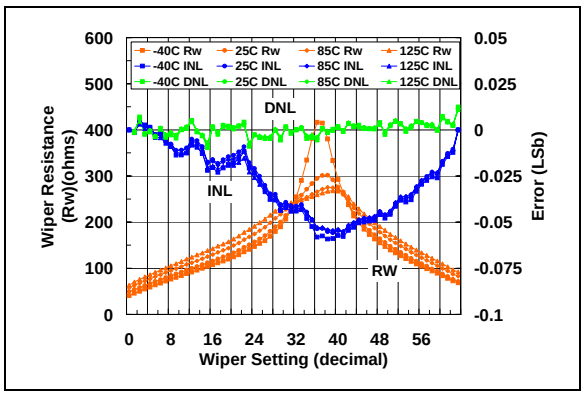


FIGURE 2-38: *50 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 2.7V).*

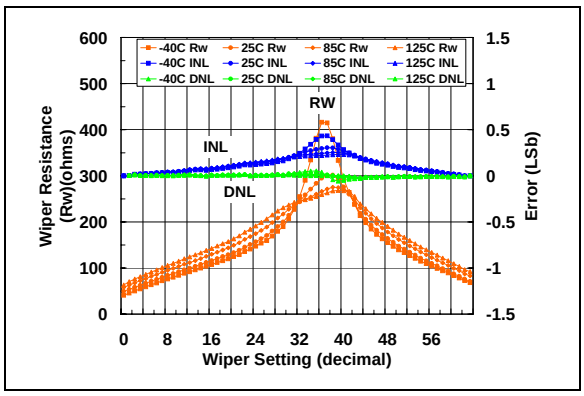


FIGURE 2-41: *50 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 2.7V).*

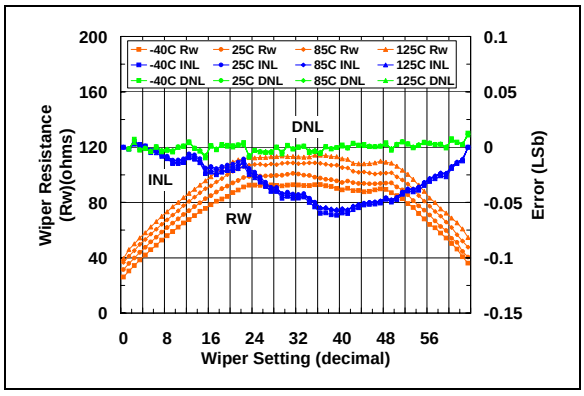


FIGURE 2-39: *50 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

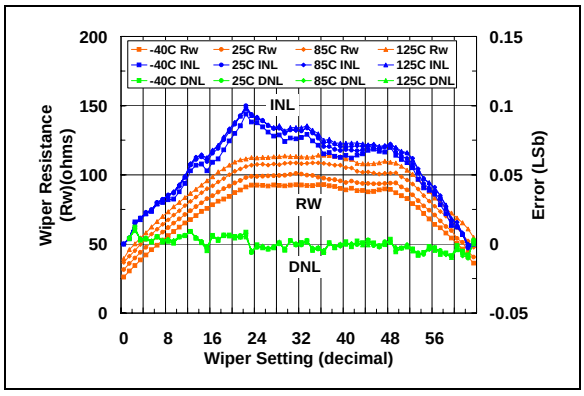


FIGURE 2-42: *50 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

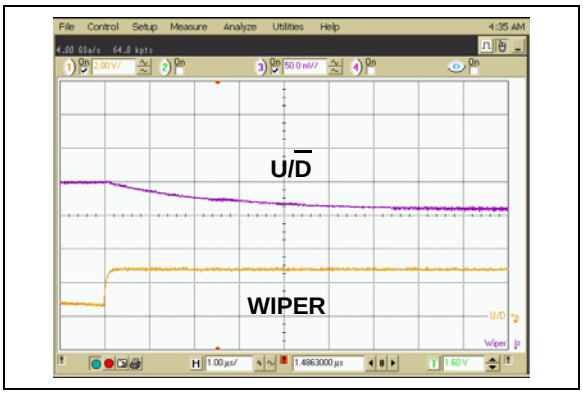


FIGURE 2-43: *50 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 2.7V).*

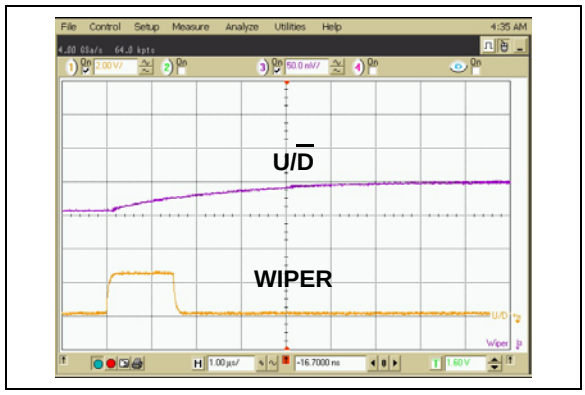


FIGURE 2-46: *50 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 2.7V).*

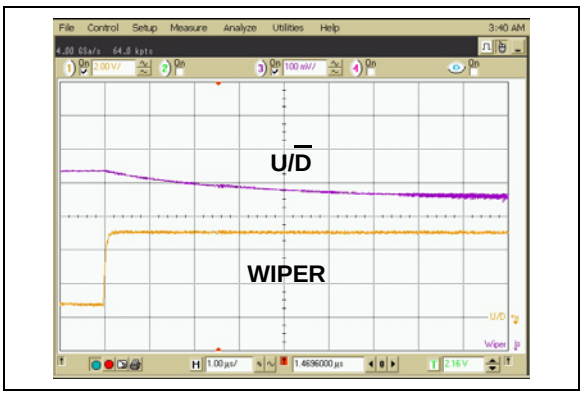


FIGURE 2-44: *50 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 5.5V).*

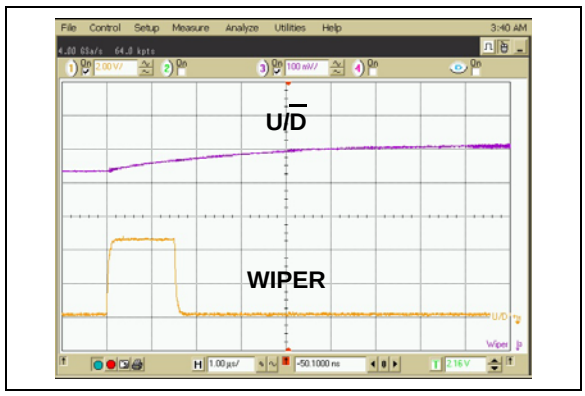


FIGURE 2-47: *50 kΩ - Low-Voltage Increment Wiper Settling Time (V_{DD} = 5.5V).*

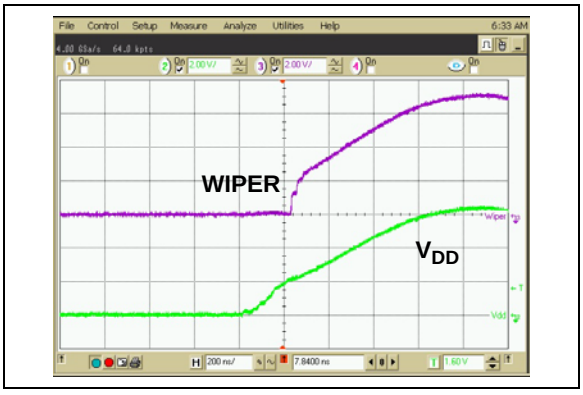


FIGURE 2-45: *50 kΩ – Power-Up Wiper Response Time.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP4021 Pin No.	MCP4022 MCP4023 Pin No.	MCP4024 Pin No.	Symbol	Function
1	1	1	V_{DD}	Positive Power Supply Input (+2.7V to +5.5V)
2	2	2	V_{SS}	Ground
3	6	—	A	Potentiometer Terminal A
4	5	5	W	Potentiometer Wiper Terminal
5	4	4	$\overline{CS}$	Chip Select Input
6	—	—	B	Potentiometer Terminal B
7	—	—	NC	No Connection
8	3	3	U/$\overline{D}$	Increment/$\overline{\text{Decrement}}$ Input

3.1 Positive Power Supply Input (V_{DD})

V_{DD} is the positive power supply input. The input power supply is relative to V_{SS} and can range from 2.7V to 5.5V. A de-coupling capacitor on V_{DD} is recommended to achieve maximum performance.

3.2 Ground (V_{SS})

V_{SS} is the analog ground pin.

3.3 Potentiometer Terminal A

Potentiometer terminal A is the fixed connection to the 0x3F terminal of the digital potentiometer. It is available on MCP4021, MCP4022 and MCP4023. Terminal A does not have a polarity relative to terminals W or B. Terminal A can support both positive and negative current. Not available on the MCP4024.

3.4 Potentiometer Wiper Terminal W

The Wiper terminal is the adjustable terminal of the digital potentiometer. It is available on all MCP4021/2/3/4 devices. The wiper does not have a polarity relative to terminals A or B. The wiper can support both positive and negative current.

3.5 Potentiometer Terminal B

Potentiometer terminal B is the fixed connection to the 0x00 terminal of the digital potentiometer. It is available on MCP4021. Terminal B is connected to V_{SS} on the MCP4023 and MCP4024. Terminal B does not have a polarity relative to terminals W or A. Terminal B can support both positive and negative current. Not available on the MCP4022.

3.6 $\overline{\text{Chip Select}}$ ($\overline{CS}$)

The $\overline{CS}$ is the chip select input, which requires an active-low signal to enable low-voltage Increment and Decrement commands. $\overline{CS}$, when driven high (> V_{PP}), will enable high-voltage increment, decrement and WiperLock technology commands.

3.7 Increment/Decrement (U/$\overline{D}$)

The U/$\overline{D}$ input is used to increment and decrement the wiper on the digital potentiometer. An increment moves the wiper one step toward terminal A. A decrement moves the wiper one step toward terminal B.

4.0 GENERAL OVERVIEW

The MCP4021/2/3/4 devices are general purpose digital potentiometers intended to be used in applications where a programmable resistance with moderate bandwidth is desired.

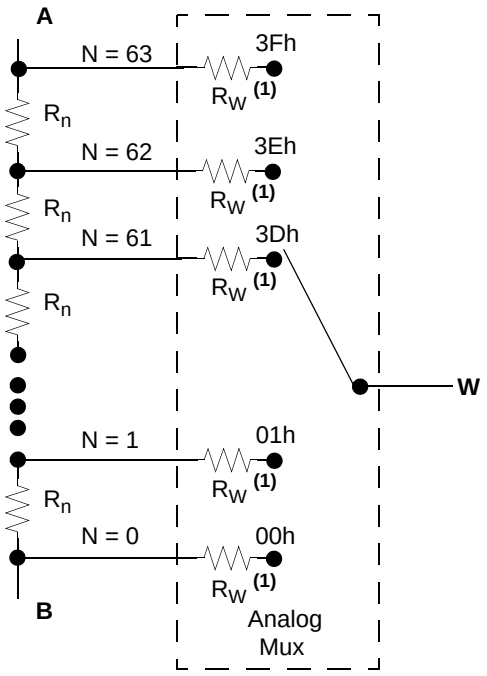
Applications generally suited for the MCP4021/2/3/4 devices include:

- Set point or offset trimming
- Sensor calibration
- Selectable gain and offset amplifier designs
- Cost-sensitive mechanical trim pot replacement

The digital potentiometer is available in four nominal resistances where the nominal resistance is defined as the resistance between terminal A and terminal B. The four nominal resistances are 2 kΩ, 5 kΩ, 10 kΩ, and 50 kΩ.

The MCP4021/2/3/4 essentially has 63 resistors in a string between terminal A and terminal B. The wiper can be set to tap onto any of these 63 resistors thus providing 64 possible settings (including terminal A and terminal B). Equation 4-1 illustrates the calculation used to determine the resistance between the wiper and terminal B.

Figure 4-1 shows a block diagram for the resistive network of the device.



Note 1: The wiper resistance is tap dependent. That is, each tap selection resistance has a small variation. This variation effects the smaller resistance devices (2 kΩ) more.

FIGURE 4-1: *Block Diagram.*

EQUATION 4-1: R_{WB} CALCULATION

$$R_{WB} = \frac{R_{AB}N}{63} + R_W$$

N = 0 to 63 (decimal)

1 LSb is the ideal resistance difference between two successive codes. If we use N = 1 and R_{wiper} = 0 in Equation 4-1, we can calculate the step size for each increment or decrement command.

4.1 Digital Interface

The MCP4021/2/3/4 utilizes a 2-wire synchronous serial protocol to increment or decrement the digital potentiometer's wiper terminal. The Increment/Decrement protocol utilizes $\overline{CS}$ and U/$\overline{D}$ inputs. Both inputs are tolerant of signals up to 12.5V without damaging the device. $\overline{CS}$ has two input buffers. A standard CMOS low-voltage input buffer and a high-voltage input buffer. This enables additional commands without requiring additional input pins. The high-voltage commands have the same functionality as the low-voltage command, and they determine the state of the nonvolatile WL bit.

4.2 The WiperLock™ Technology

The WiperLock technology enables a feature that prevents the wiper setting from being incremented or decremented by low-voltage serial commands. This also prevents writes to the nonvolatile memory with low-voltage commands. Enabling and disabling the WiperLock technology feature requires high-voltage commands. Incrementing and decrementing the wiper requires high-voltage commands when the feature is enabled. The high voltage threshold is intended to prevent the wiper setting from being altered by noise or intentional low-voltage transitions on U/$\overline{D}$ and $\overline{CS}$, while still providing flexibility for production or calibration environments.

4.3 Power Supply Considerations

The typical application will require a bypass capacitor in order to filter high-frequency noise, which can be induced onto the power supply's traces. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity. Figure 4-2 illustrates an appropriate bypass strategy.

In this example, the recommended bypass capacitor value is 0.1 µF. This capacitor should be placed as close to the device power pin (V_{DD}) as possible (within 4 mm).

The power source supplying these devices should be as clean as possible. If the application circuit has separate digital and analog power supplies, V_{DD} and V_{SS} should reside on the analog plane.

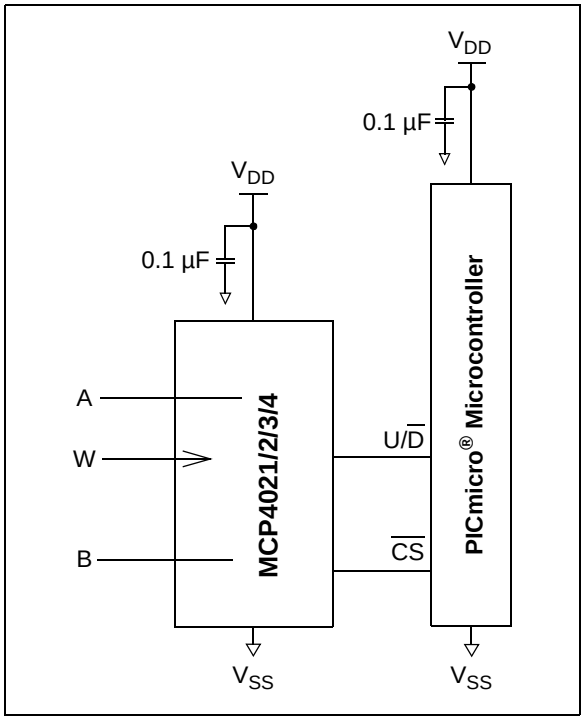


FIGURE 4-2: *Typical Microcontroller Connections.*

4.4 Layout Considerations

Inductively-coupled AC transients and digital switching noise can degrade the input and output signal integrity, potentially masking the MCP4021/2/3/4's performance. Careful board layout will minimize these effects and increase the Signal-to-Noise Ratio (SNR). Bench testing has shown that a multi-layer board utilizing a low-inductance ground plane, isolated inputs, isolated outputs and proper decoupling are critical to achieving the performance that the silicon is capable of providing. Particularly harsh environments may require shielding of critical signals.

If low noise is desired, breadboards and wire-wrapped boards are not recommended.

4.5 Accuracy

4.5.1 INL

INL error for these devices is the maximum deviation between an actual code transition point and its corresponding ideal transition point once offset and gain errors have been removed. These endpoints are from 0x00 to 0x3F. Refer to Figure 4-3.

Positive INL means higher resistance than ideal. Negative INL means lower resistance than ideal.

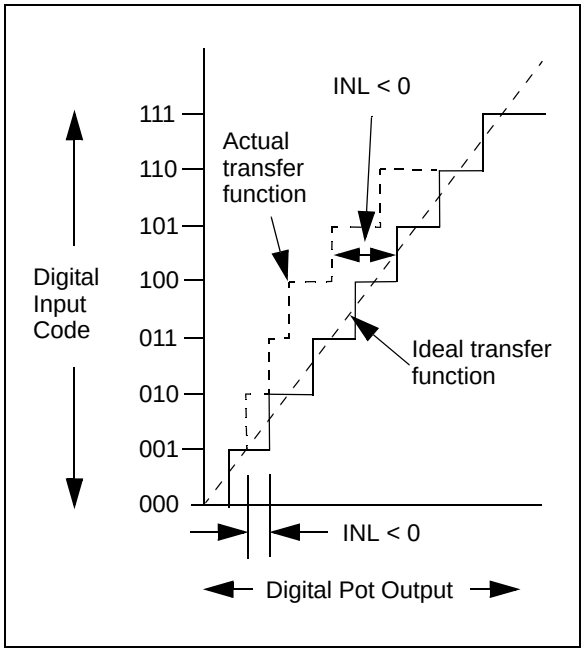


FIGURE 4-3: *INL Accuracy.*

4.5.2 DNL ACCURACY

DNL error is the measure of variations in code widths from the ideal code width. A DNL error of zero would imply that every code is exactly 1 LSb wide.

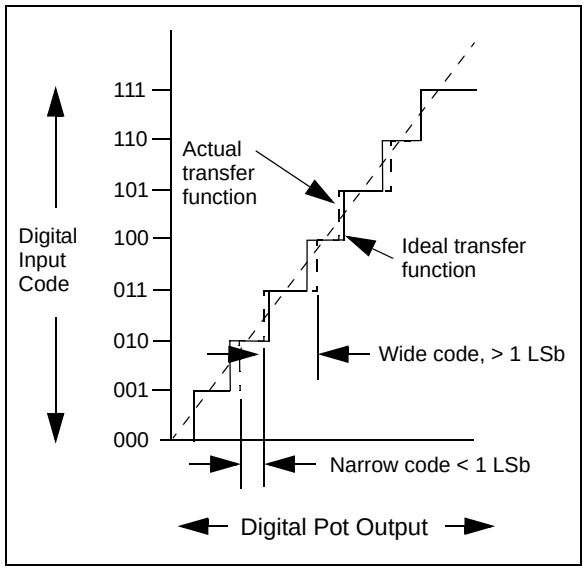


FIGURE 4-4: *DNL Accuracy.*

4.5.3 RATIOMETRIC TEMPERATURE COEFFICIENT

The ratiometric temperature coefficient quantifies the error in the ratio R_{AW}/R_{WB} due to temperature drift. This is typically the critical error when using a potentiometer device (MCP4021 and MCP4023) in a voltage divider configuration.

4.5.4 ABSOLUTE TEMPERATURE COEFFICIENT

The absolute temperature coefficient quantifies the error in the end-to-end resistance (Nominal resistance R_{AB}) due to temperature drift. This is typically the critical error when using a rheostat device (MCP4022 and MCP4024) in an adjustable resistor configuration.

4.5.5 WIPER RESISTANCE

Wiper resistance is the series resistance of the wiper. This resistance is typically measured when the wiper is positioned at either zero-scale (00h) or full-scale (3Fh). The wiper resistance in potentiometer-generated voltage divider applications is not a significant source of error. The wiper resistance in rheostat applications can create significant nonlinearity as the wiper is moved toward zero-scale (00h). The lower the nominal resistance, the greater the possible error.

4.6 Power-up and Brown Out

The MCP4021/2/3/4 does not allow writes to its EEPROM, while V_{DD} is below the V_{WP} threshold.

The wiper state when $V_{DD} < V_{WP}$ is unknown.

When $V_{WP} < V_{DD} < V_{min}$ (2.7V), the electrical performance may not meet the data sheet specifications. In this region, the wiper will be initialized to the value stored in the EEPROM and the device may be capable of incrementing, decrementing and writing to its EEPROM if the proper command is executed.

The MCP4021/2/3/4 will electrically function as specified by the electrical specifications when $V_{DD} > 2.7V$.

4.6.1 STANDBY MODE

Standby mode is entered any time $\overline{CS}$ is above V_{IL}, below V_{PP} and all write cycles are completed.

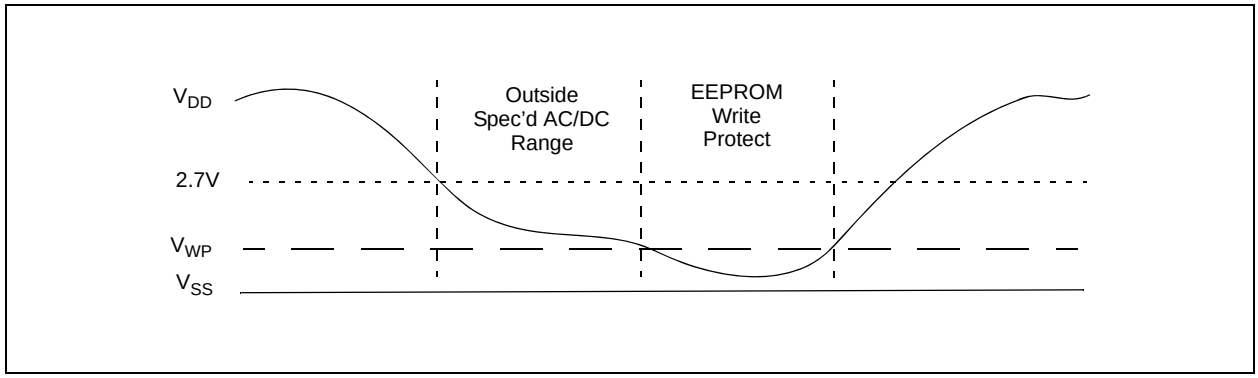


FIGURE 4-5: *Power-up and Brown-out.*

5.0 SERIAL INTERFACE

5.1 Overview

The MCP4021/2/3/4 utilizes a simple 2-wire interface to increment or decrement the digital potentiometer's wiper terminal (W), store the wiper setting in nonvolatile memory and turn the WiperLock technology feature on or off. The two signals are $\overline{CS}$ and U/$\overline{D}$. $\overline{CS}$ is the $\overline{Chip}$ Select input, while U/$\overline{D}$ is the Up/$\overline{Down}$ input.

The Increment/Decrement protocol enables the device to move one step at a time through the range of possible resistance values. The wiper value is initialized with the value stored in the internal EEPROM upon power-up. A wiper value of 0h connects the wiper to terminal B. A wiper value of 3Fh connects the wiper to terminal A. Increment commands move the wiper toward terminal A, but will not increment to a value greater than 3Fh. Decrement commands move the wiper toward terminal B, but will not decrement below 00h.

Two types of commands are low-voltage and high-voltage commands. The type of command is defined by the level $\overline{CS}$ is driven to. If $\overline{CS}$ is driven from V_{DD} to < V_{IL}, a low-voltage Command is selected. High-voltage commands are selected if $\overline{CS}$ is driven from V_{DD} to > V_{PP}.

Refer to **Section 1.0 "Electrical Characteristics"**, AC/DC Electrical Characteristics table for detailed input threshold and timing specifications.

Communication is unidirectional and, thus, data cannot be directly read out of the MCP4021/2/3/4.

5.2 Low-Voltage Commands

5.2.1 INCREMENT WITH THE WIPERLOCK TECHNOLOGY FEATURE DISABLED

Entering Increment mode is achieved by initializing U/$\overline{D}$ to a high state prior to achieving a low state on $\overline{CS}$. Subsequent rising edges of U/$\overline{D}$ will increment the wiper setting (toward terminal A). Refer to Figures 5-1 and 5-2.

5.2.2 DECREMENT WITH THE WIPERLOCK TECHNOLOGY FEATURE DISABLED

Entering Decrement mode is achieved by initializing the U/$\overline{D}$ signal to a low state prior to achieving a low state on $\overline{CS}$. Subsequent rising edges of U/$\overline{D}$ will decrement the wiper setting (toward terminal B). Refer to Figures 5-3 and 5-4.

The MCP4021/2/3/4 has the unique feature of allowing the user to determine whether or not to "save" the wiper state to its internal EEPROM memory by selecting the state of U/$\overline{D}$ when $\overline{CS}$ transitions back to a high state (V_{DD}). Simply, if U/$\overline{D}$ is not at the same state when $\overline{CS}$ transitions high as it was when $\overline{CS}$ transitioned low, the wiper setting will be written to internal EEPROM.

5.2.3 EXAMPLES OF THE 5 POSSIBLE LOW-VOLTAGE COMMANDS

1. If the U/$\overline{D}$ signal is low when ending Decrement mode, the EEPROM will remain unchanged and the device will be capable of reentering an Increment/Decrement mode immediately since the 5 ms write cycle was not started. See Figure 5-1.
2. If the U/$\overline{D}$ signal is high when ending Decrement mode, the current wiper value will be written to the internal EEPROM. See Figure 5-2.
3. If the U/$\overline{D}$ signal is high when ending Increment Mode, the EEPROM will remain unchanged and the device will be capable of re-entering an Increment/Decrement Mode immediately since the 5 ms write cycle was not started. See Figure 5-3.
4. If the U/$\overline{D}$ signal is low when ending Increment mode, the current wiper value will be written to the internal EEPROM. See Figure 5-4.
5. U/$\overline{D}$ can be dropped after Increment mode has been latched. While this will not increment the wiper (requires a rising edge), it will write the existing wiper setting to the internal EEPROM once $\overline{CS}$ is raised. This is useful as a "save wiper" command without changing the wiper setting. See Figure 5-5.

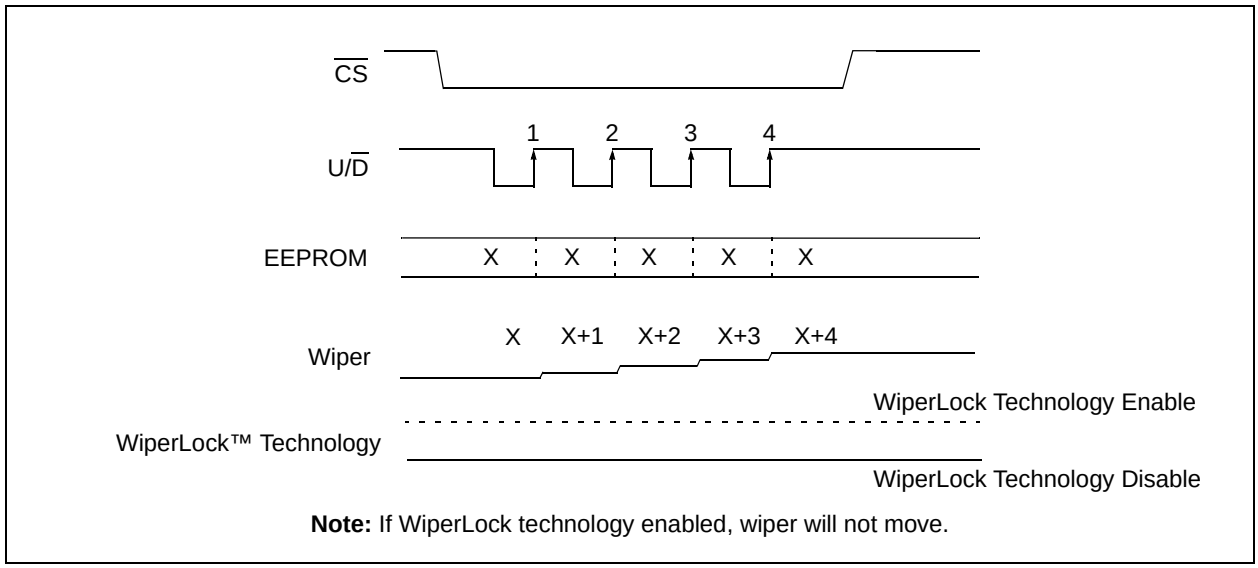


FIGURE 5-1: *Low-Voltage Increment without Saving Wiper to EEPROM.*

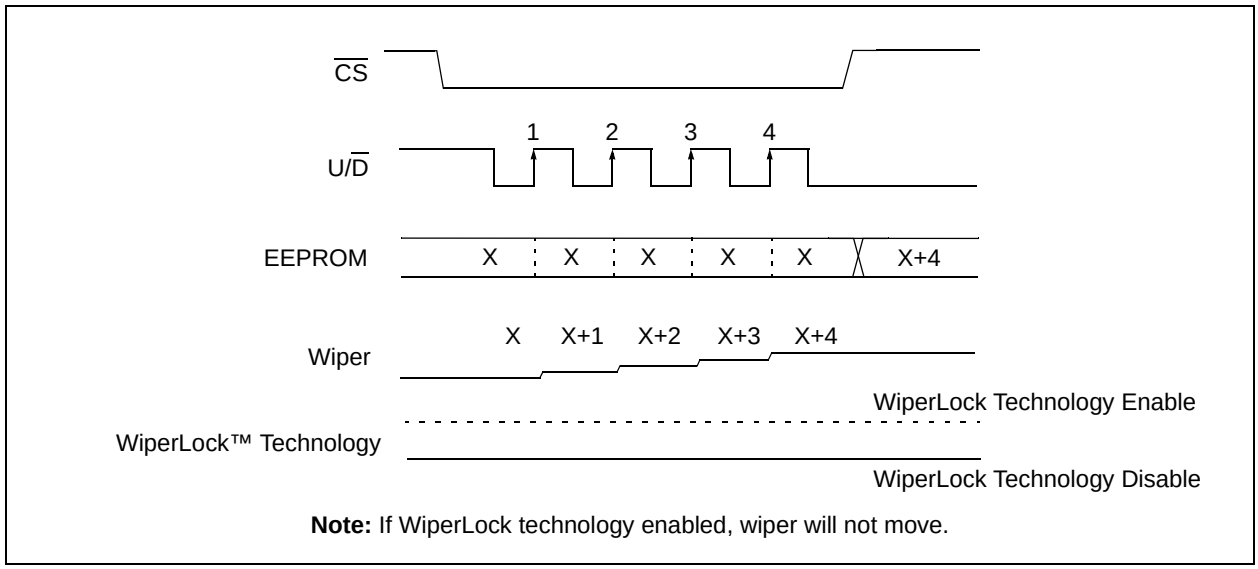
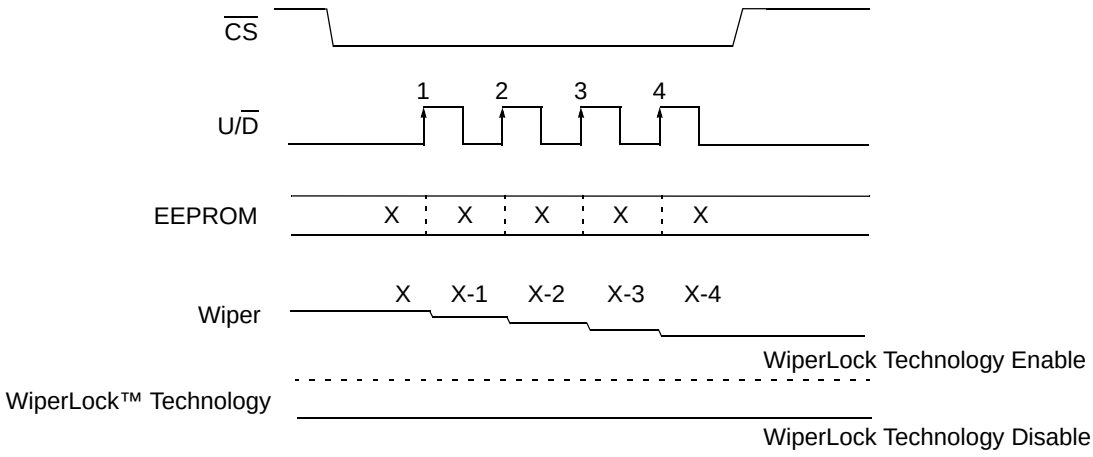
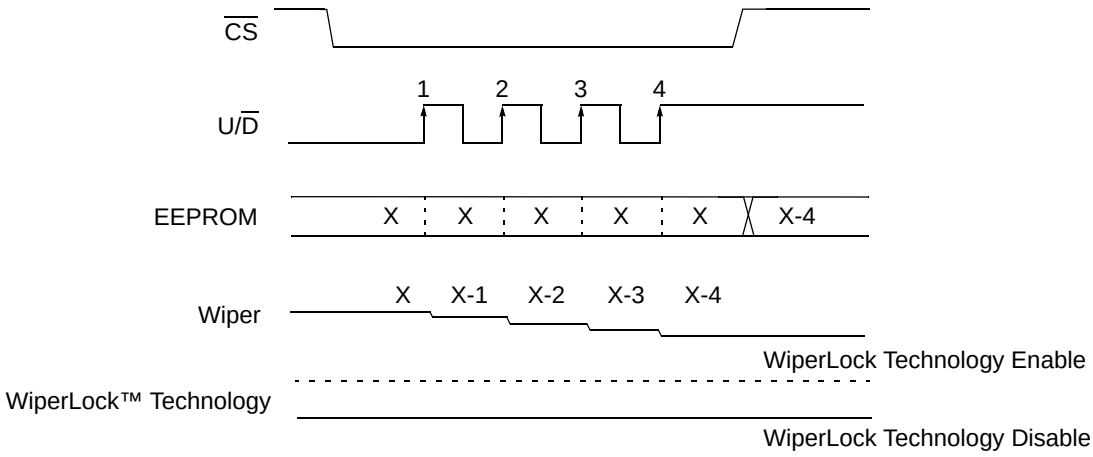


FIGURE 5-2: *Low-Voltage Increment with Write of Wiper Setting to EEPROM.*



Note: If WiperLock technology enabled, wiper will not change.

FIGURE 5-3: *Low-Voltage Decrement without Saving Wiper to EEPROM.*



Note: If WiperLock technology enabled, wiper will not change.

FIGURE 5-4: *Low-Voltage Decrement with Write of Wiper Setting to EEPROM.*

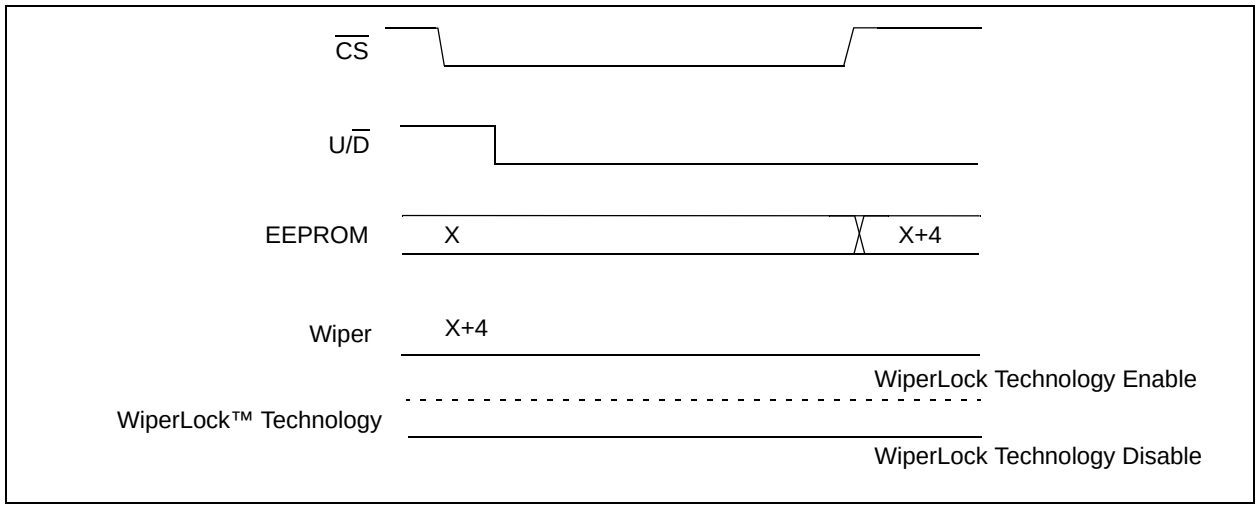


FIGURE 5-5: *Low-Voltage Write of Wiper Setting to EEPROM without Increment/Decrement of Wiper.*

5.3 High-Voltage Commands

The low-voltage increment/decrement commands are basically identical to the high-voltage increment/decrement commands except that $\overline{CS}$ is driven above V_{PP} instead of below V_{IL}. High-voltage commands will increment/decrement the wiper regardless of the status of the WiperLock technology. An EEPROM write cycle will always occur on the falling edge of $\overline{CS}$.

The MCP4021/2/3/4 has the unique feature of allowing the user to determine whether or not to "lock" or "unlock" the wiper state using the state of the U/$\overline{D}$ signal when $\overline{CS}$ falls below V_{PP}. Simply, if U/$\overline{D}$ is not at the same state when $\overline{CS}$ transitions low as it was when $\overline{CS}$ transitioned high, the WiperLock technology feature will be enabled.

5.3.1 INCREMENT AND DISABLE THE WIPERLOCK TECHNOLOGY FEATURE

Entering Increment mode is achieved by initializing U/$\overline{D}$ to a high state prior to $\overline{CS}$ achieving >V_{PP}. Subsequent rising edges of U/$\overline{D}$ will increment the wiper setting (toward terminal A). Setting U/$\overline{D}$ to a high state prior to $\overline{CS}$ returning to V_{DD} will begin a write cycle and disable the WiperLock technology feature. See Figure 5-6.

5.3.2 INCREMENT AND ENABLE THE WIPERLOCK TECHNOLOGY FEATURE

Entering Increment mode is achieved by initializing U/$\overline{D}$ to a high state prior to $\overline{CS}$ achieving > V_{PP}. Subsequent rising edges of U/$\overline{D}$ will increment the wiper setting (toward terminal A). Setting U/$\overline{D}$ to a low state prior to $\overline{CS}$ returning to V_{DD} will begin a write cycle and enable the WiperLock technology feature. See Figure 5-7.

5.3.3 DECREMENT AND DISABLE THE WIPERLOCK TECHNOLOGY FEATURE

Entering Decrement mode is achieved by initializing U/$\overline{D}$ to a low state prior to $\overline{CS}$ achieving > V_{PP}. Subsequent rising edges of U/$\overline{D}$ will decrement the wiper setting (toward terminal B). Setting U/$\overline{D}$ to a low state prior to $\overline{CS}$ returning to V_{DD} will begin a write cycle and disable the WiperLock technology feature. See Figure 5-8.

5.3.4 DECREMENT AND ENABLE THE WIPERLOCK TECHNOLOGY FEATURE

Entering Decrement mode is achieved by initializing U/$\overline{D}$ to a low state prior to $\overline{CS}$ achieving > V_{PP}. Subsequent rising edges of U/$\overline{D}$ will decrement the wiper setting (toward terminal B). Setting U/$\overline{D}$ to a high state prior to $\overline{CS}$ returning to V_{DD} will begin a write cycle and enable the WiperLock technology feature. See Figure 5-9.

5.3.5 DISABLE THE WIPERLOCK TECHNOLOGY FEATURE WITHOUT INCREMENT OR DECREMENT

Enter either the High-Voltage (HV) Increment or Decrement modes, but do not alter U/$\overline{D}$ prior to $\overline{CS}$ transitioning back below V_{PP}. This will disable the WiperLock technology feature and store the existing wiper value. See Figure 5-10.

5.3.6 ENABLE THE WIPERLOCK TECHNOLOGY FEATURE WITHOUT INCREMENT OR DECREMENT

U/$\overline{D}$ can be dropped after HV Increment mode has been latched. This will not increment the wiper (requires a rising edge), but will cause an Erase/Write (E/W) cycle when $\overline{CS}$ falls below V_{PP}. This will enable the WiperLock technology feature and store the existing wiper value. See Figure 5-11.

Note:	A rising edge (> V_{PP}) on $\overline{CS}$ during an E/W cycle will be ignored. Adequate delay must be allowed after a write cycle is started since there is no way to determine exactly when an E/W cycle has completed.

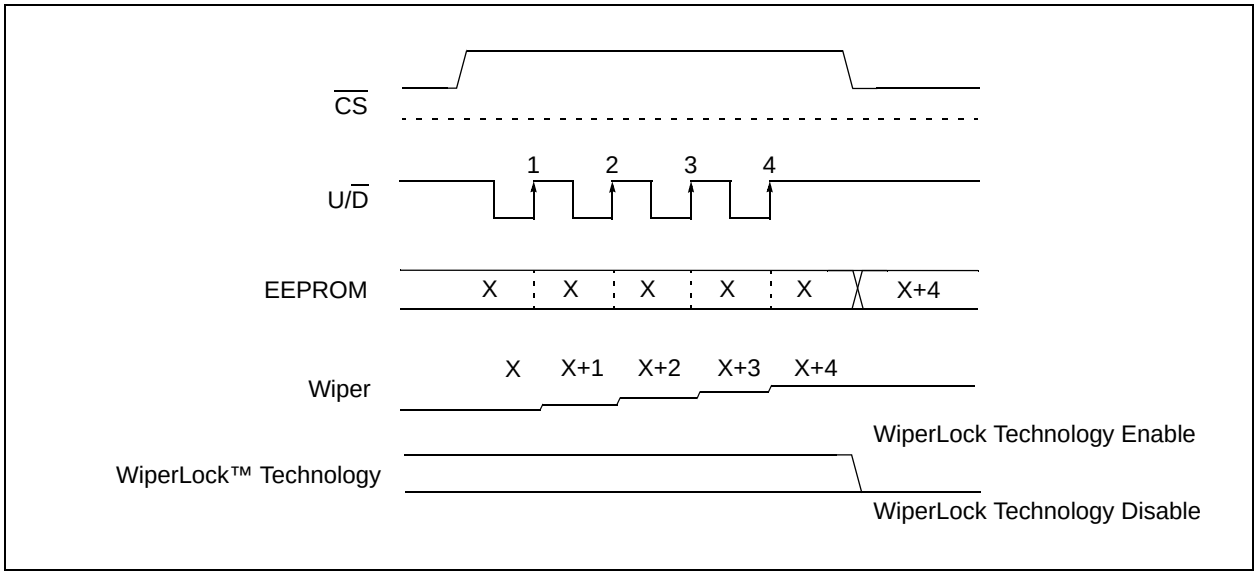


FIGURE 5-6: *High-Voltage Increment with the WiperLock™ Technology Disabled.*

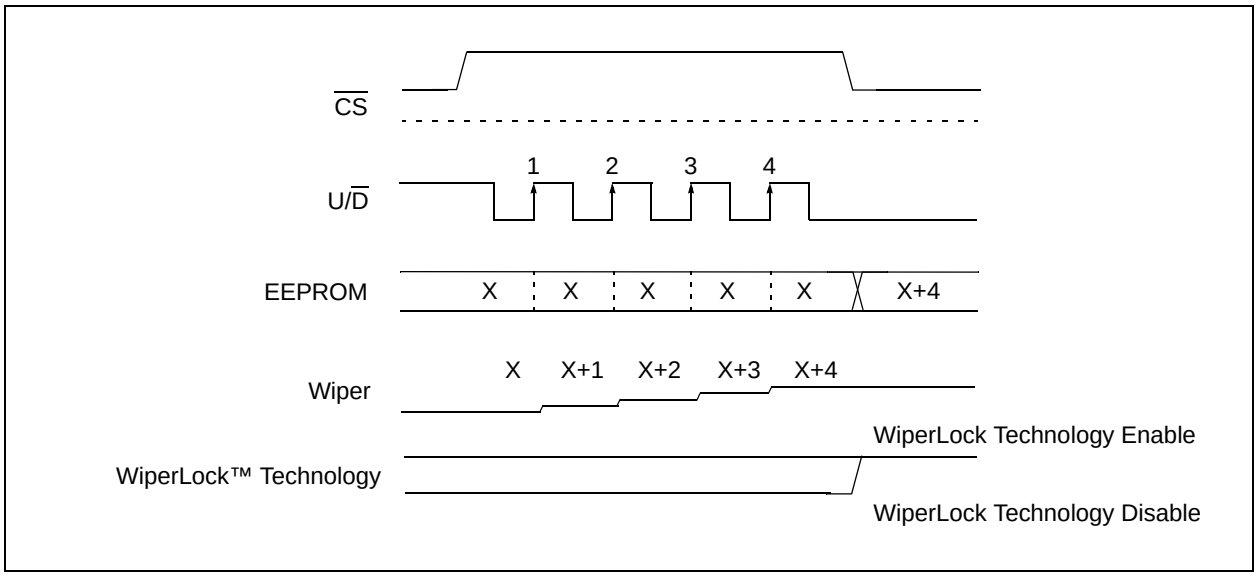


FIGURE 5-7: *High-Voltage Increment with the WiperLock™ Technology Enabled.*

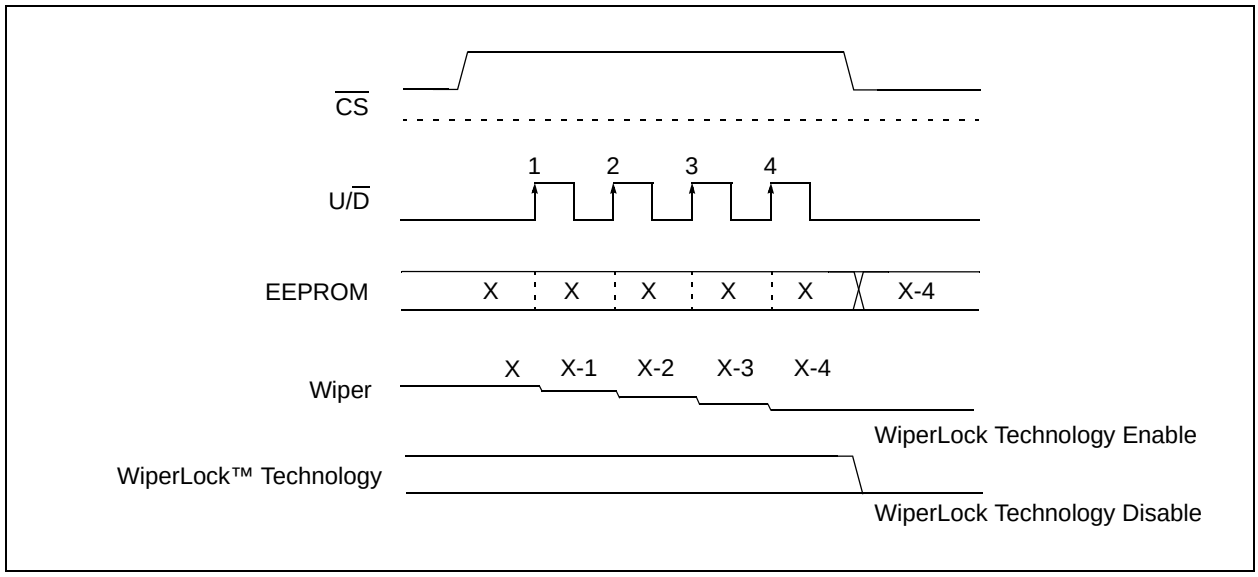


FIGURE 5-8: *High-Voltage Decrement with the WiperLock™ Technology Disabled.*

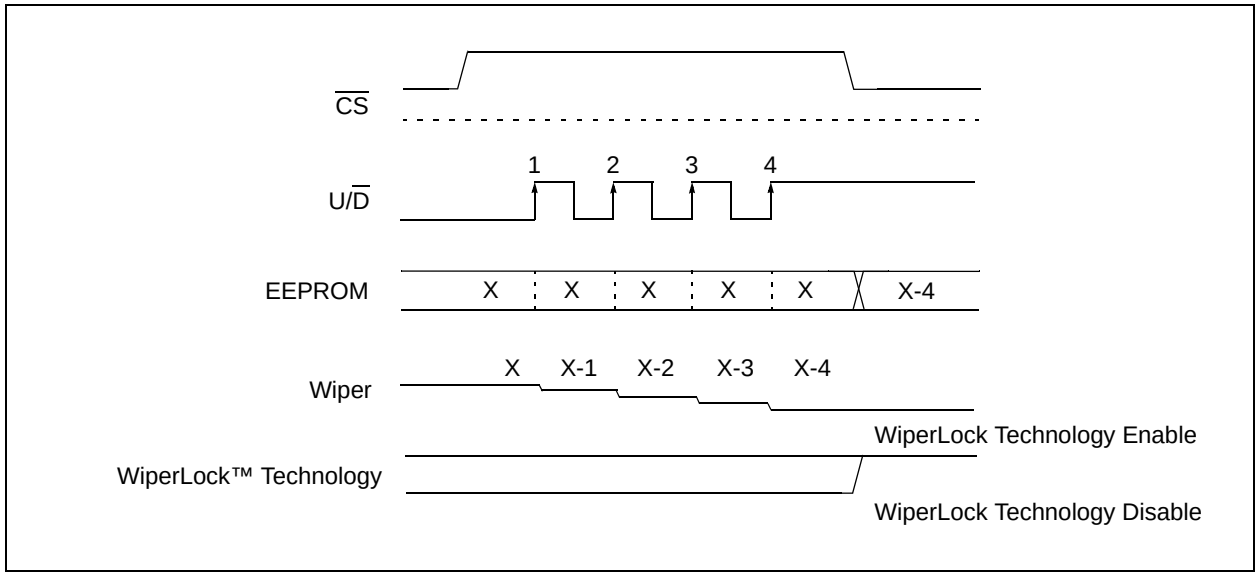


FIGURE 5-9: *High-Voltage Decrement with the WiperLock™ Technology Enabled.*

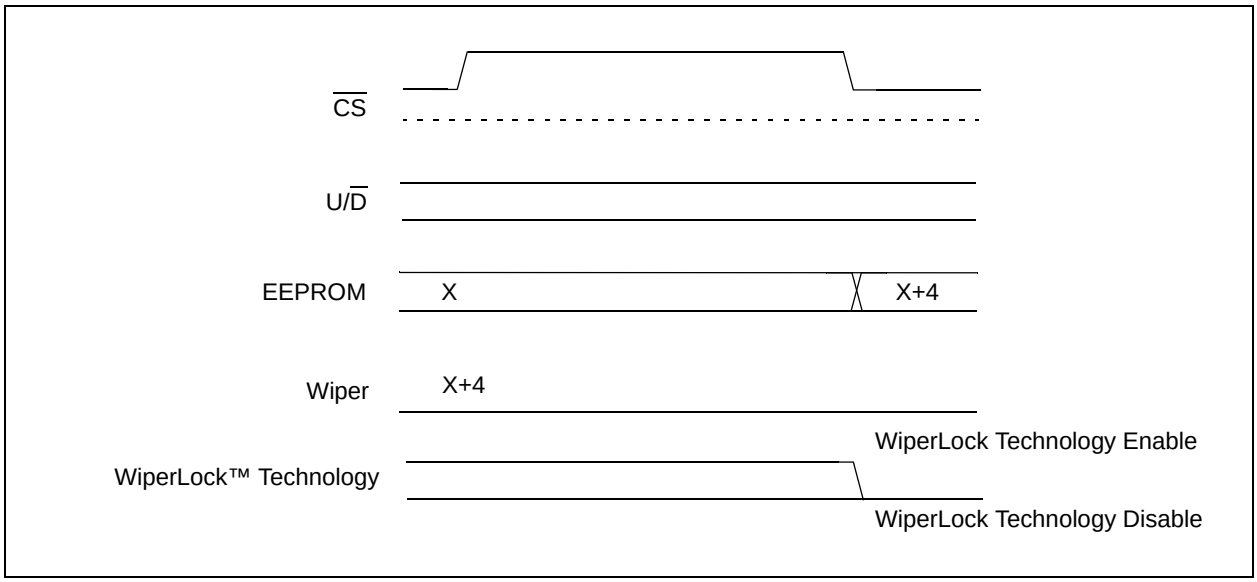


FIGURE 5-10: *High-Voltage Disable of the WiperLock™ Technology without Increment or Decrement of Wiper.*

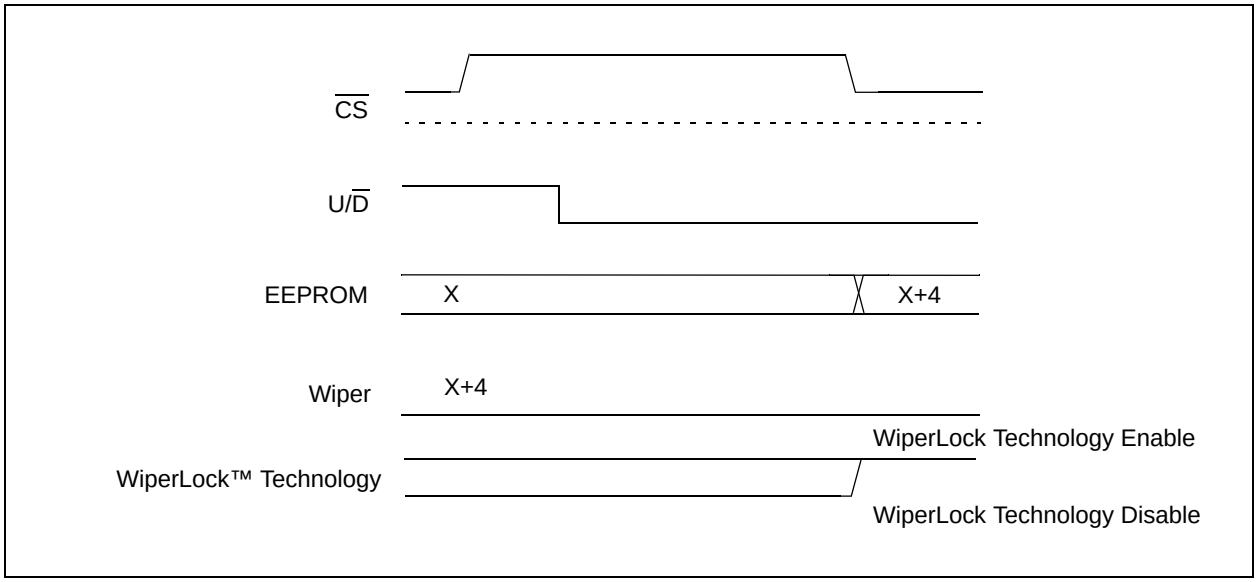


FIGURE 5-11: *High-Voltage Enable of the WiperLock™ Technology without Increment or Decrement of Wiper.*

6.0 TYPICAL APPLICATIONS

Nonvolatile digital potentiometers have a multitude of practical uses in modern electronic circuits. The most popular uses include precision calibration of set point thresholds, sensor trimming, LCD bias trimming, audio attenuation, adjustable power supplies, motor control overcurrent trip setting, adjustable gain amplifiers and offset trimming. The MCP4021/2/3/4 can be used to replace the common mechanical trim pot in applications where the operating and terminal voltages are within CMOS process limitations (V_{DD} = 2.7V to 5.5V).

6.1 Set Point Threshold Trimming

Applications that need accurate detection of an input threshold event often need several sources of error eliminated. Use of comparators and operational amplifiers (op amps) with low offset and gain error can help achieve the desired accuracy, but in many applications, the input source variation is beyond the designer's control. If the entire system can be calibrated after assembly in a controlled environment (like factory test), these sources of error are minimized if not entirely eliminated.

Figure 6-1 illustrates a common digital potentiometer configuration. This configuration is often referred to as a "windowed voltage divider". Note that R_1 and R_2 are not necessary to create the voltage divider, but their presence is useful when the desired threshold has limited range. It is "windowed" because R_1 and R_2 can narrow the adjustable range of V_{TRIP} to a value much less than $V_{DD} - V_{SS}$. If the output range is reduced, the magnitude of each output step is reduced. This effectively increases the trimming resolution for a fixed digital potentiometer resolution. This technique may allow a lower-cost digital potentiometer to be utilized (64 steps instead of 256 steps).

The MCP4021/2/3/4's low DNL performance is critical to meeting calibration accuracy in production without having to use a higher precision digital potentiometer.

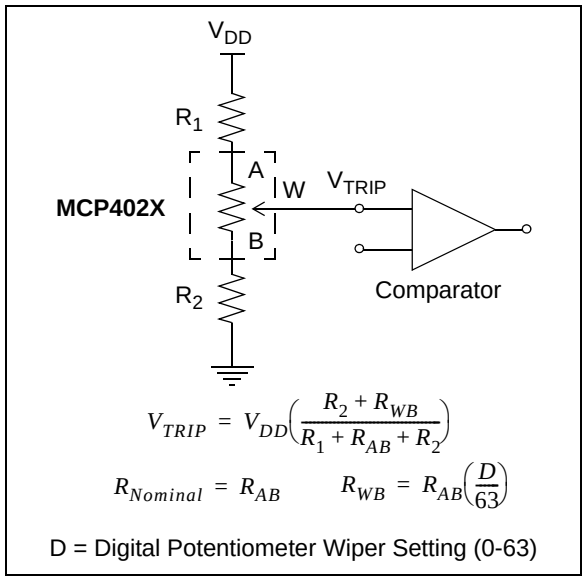


FIGURE 6-1: *Using the Digital Potentiometer to Set a Precision Threshold.*

6.1.1 TRIMMING A THRESHOLD FOR AN OPTICAL SENSOR

If the application has to calibrate the threshold of a diode, transistor or resistor, a variation range of 0.1V is common. Often, the desired a resolution of 2 mV or better is adequate to accurately detect the presence of a precise signal. A windowed voltage divider, utilizing the MCP4021/2/3/4, would be a potential solution. Figure 6-2 illustrates this example application.

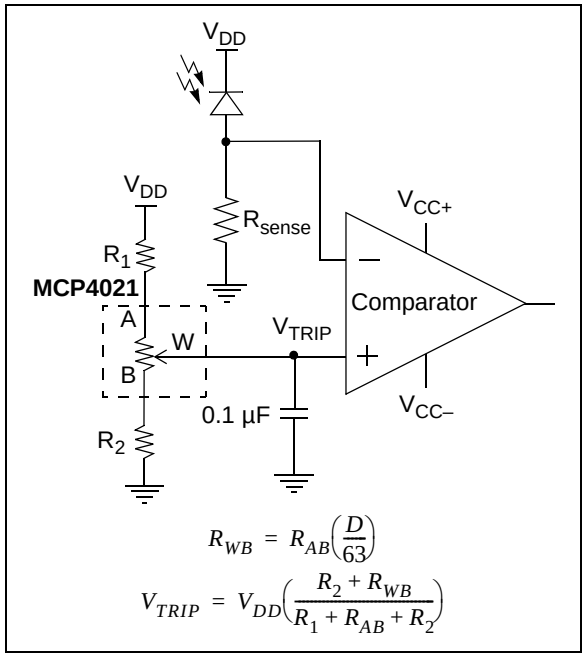


FIGURE 6-2: *Set Point or Threshold Calibration.*

6.2 Operational Amplifier Applications

Figure 6-3, Figure 6-4 and Figure 6-5 illustrate typical amplifier circuits that could replace fixed resistors with the MCP4021/2/3/4 to achieve digitally-adjustable analog solutions.

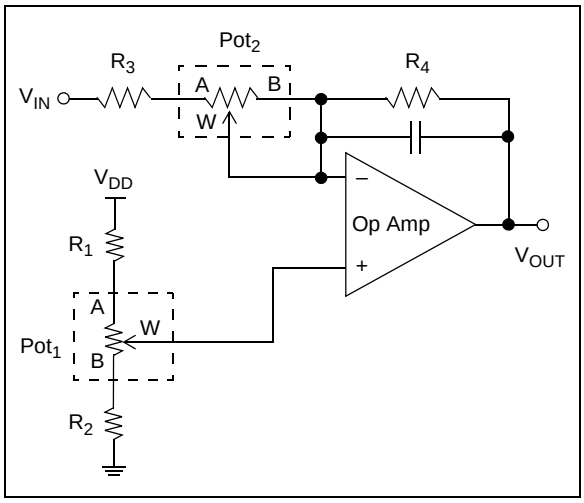


FIGURE 6-3: *Trimming Offset and Gain in an Inverting Amplifier Using a Digital Potentiometer.*

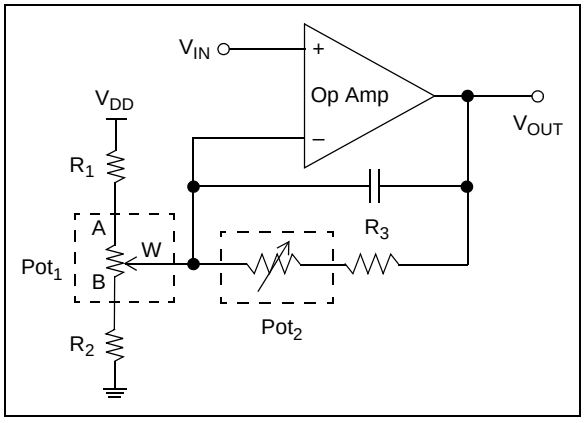


FIGURE 6-4: *Trimming Offset and Gain in a Non-Inverting Amplifier Using a Digital Potentiometer.*

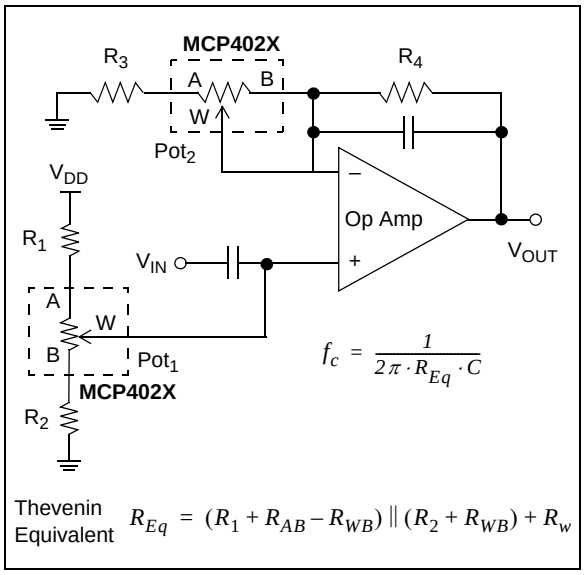


FIGURE 6-5: *Programmable Filter using a Digital Potentiometer.*

6.3 Temperature Sensor Applications

Thermistors are resistors with very predictable variation with temperature. Thermistors are a popular sensor choice when a low-cost temperature-sensing solution is desired. Unfortunately, thermistors have non-linear characteristics that are undesirable, typically requiring trimming in an application to achieve greater accuracy. There are several common solutions to trim & linearize thermistors. Figure 6-6 and Figure 6-7 are simple methods for linearizing a 3-terminal NTC thermistor. Both are simple voltage dividers using a Positive Temperature Coefficient (PTC) resistor (R_1) with a transfer function capable of compensating for the linearity error in the Negative Temperature Coefficient (NTC) thermistor.

The circuit, illustrated by Figure 6-6, utilizes a digital rheostat for trimming the offset error caused by the thermistor's part-to-part variation. This solution puts the digital potentiometer's R_W into the voltage divider calculation. The MCP4021/2/3/4's R_{AB} temperature coefficient is a low 50 ppm (-20°C to 70°C). R_W's error is substantially greater than R_{AB}'s error because R_W varies with V_{DD}, wiper setting and temperature. For the 50 kΩ devices, the error introduced by R_W is, in most cases, insignificant as long as the wiper setting is > 6. For the 2 kΩ devices, the error introduced by R_W is significant because it is a higher percentage of R_{WB}. For these reasons, the circuit illustrated in Figure 6-6 is not the most optimum method for "exciting" and linearizing a thermistor.

The circuit illustrated by Figure 6-7 utilizes a digital potentiometer for trimming the offset error. This solution removes R_W from the trimming equation along with the error associated with R_W. R_2 is not required, but can be utilized to reduce the trimming "window" and reduce variation due to the digital pot's R_{AB} part-to-part variability.

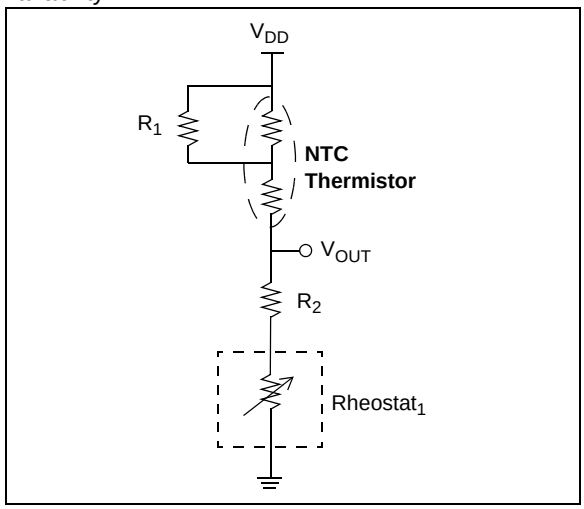


FIGURE 6-6: *Thermistor Calibration using a Digital Potentiometer in a Rheostat Configuration.*

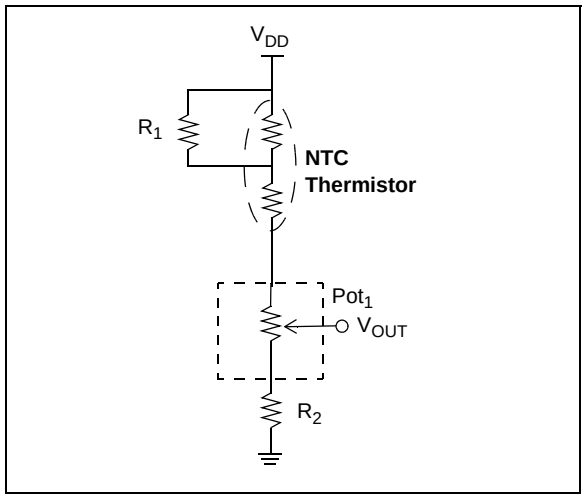


FIGURE 6-7: *Thermistor Calibration using a Digital Potentiometer in a Potentiometer Configuration.*

6.4 Wheatstone Bridge Trimming

Another common configuration to "excite" a sensor (such as a strain gauge, pressure sensor or thermistor) is the wheatstone bridge configuration. The wheatstone bridge provides a differential output instead of a single-ended output. Figure 6-8 illustrates a wheatstone bridge utilizing one to three digital potentiometers. The digital potentiometers in this example are used to trim the offset and gain of the wheatstone bridge.

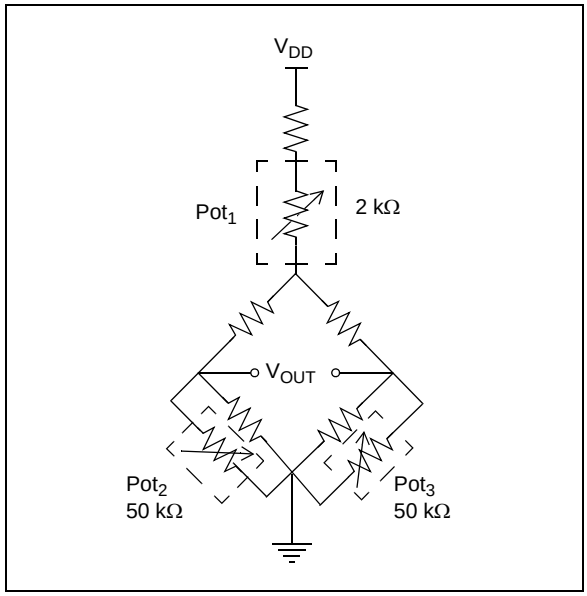


FIGURE 6-8: *Wheatstone Bridge Trimming Example using Digital Potentiometers.*

7.0 DEVELOPMENT SUPPORT

7.1 Evaluation/Demonstration Boards

The low-cost MCP402XEV board is a simple demonstration board utilizing a PIC10F206 and any desired MCP4021/2/3/4 device in a SOT-23-5, SOT-23-6 or 150 mil SOIC 8-pin package. This board has two buttons to control when the PICmicro® microcontroller generates both low- and high-voltage increment and decrement commands. The WiperLock technology enable/disable is achieved using the HV commands. Refer to www.microchip.com for more information on how to purchase and utilize the MCP402XEV board.

The SOT-23-5/6 Evaluation Board (VSUPEV2) can be used to evaluate the characteristics of the MCP4022, MCP4023 and MCP4024 devices.

The 8-pin SOIC/MSOP/TSSOP/DIP Evaluation Board (SOIC8EV) can be used to evaluate the characteristics of the MCP4021 device in either the SOIC or MSOP package.

These boards may be purchased directly from the Microchip web site at www.microchip.com.

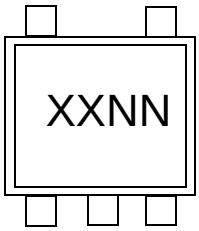
7.2 Application Notes and Tech Briefs

Application notes illustrating the performance and implementation of the MCP4021/2/3/4 are planned though not currently released. Refer to www.microchip.com for further information.

8.0 PACKAGING INFORMATION

8.1 Package Marking Information

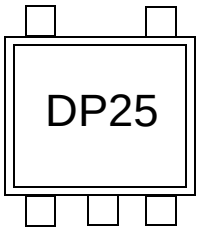
5-Lead SOT-23 (**MCP4024**)



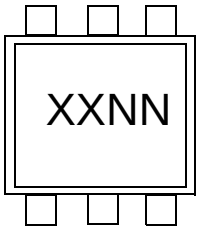
Part Number	Code
MCP4024T-202	DPNN
MCP4024T-502	DQNN
MCP4024T-103	DRNN
MCP4024T-503	DSNN

Note: Applies to 5-Lead SOT-23

Example:



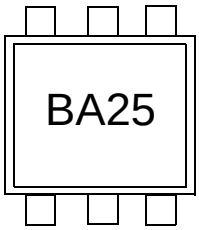
6-Lead SOT-23 (**MCP4022 / MCP4023**)



Part Number	Code
MCP4022T-202	BANN
MCP4022T-502	BBNN
MCP4022T-103	BCNN
MCP4022T-503	BDNN
MCP4023T-202	BENN
MCP4023T-502	BFNN
MCP4023T-103	BGNN
MCP4023T-503	BHNN

Note: Applies to 6-Lead SOT-23

Example:

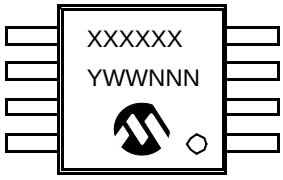


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

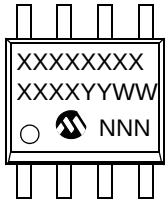
Package Marking Information (Continued)

8-Lead MSOP

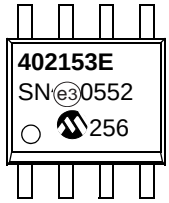


Example:

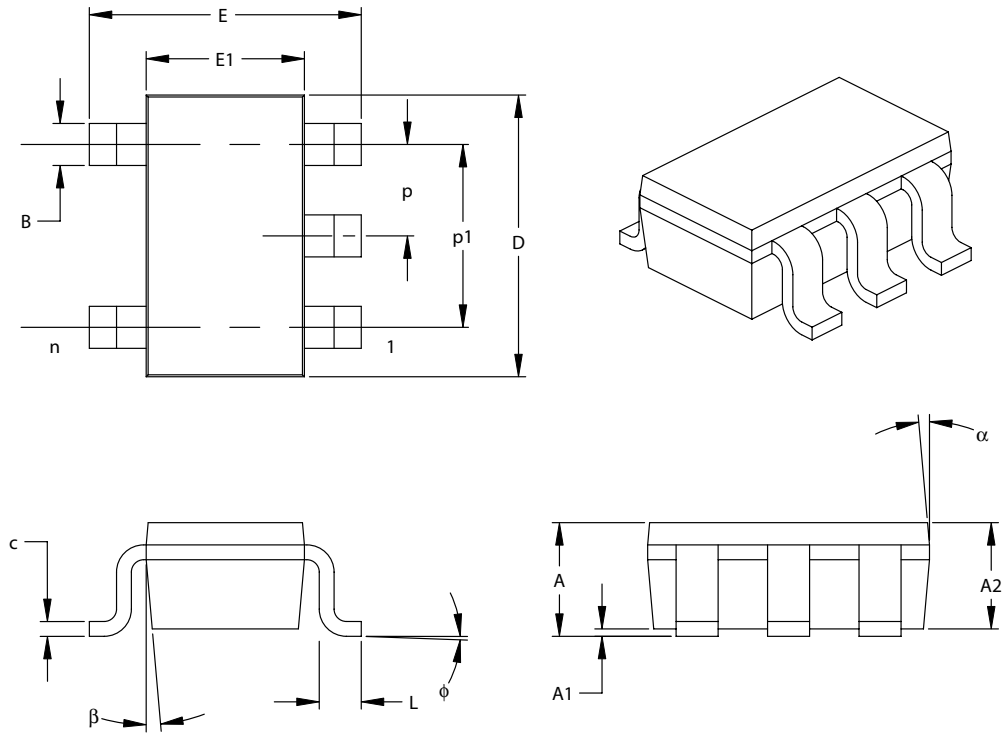
8-Lead SOIC (150 mil)



Example:



5-Lead Plastic Small Outline Transistor (OT) (SOT-23)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		5			5	
Pitch	p		.038			0.95	
Outside lead pitch (basic)	p1		.075			1.90	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	ϕ	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

*Controlling Parameter

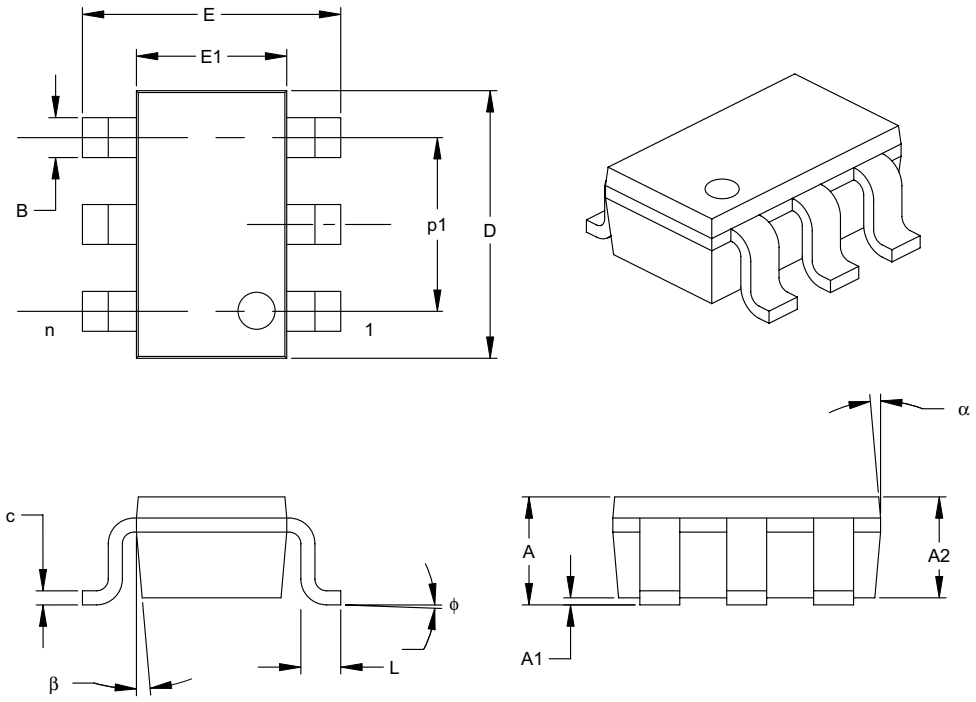
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

EIAJ Equivalent: SC-74A

Drawing No. C04-091

6-Lead Plastic Small Outline Transistor (CH) (SOT-23)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		6			6	
Pitch	p		.038			0.95	
Outside lead pitch (basic)	p1		.075			1.90	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	φ	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

*Controlling Parameter

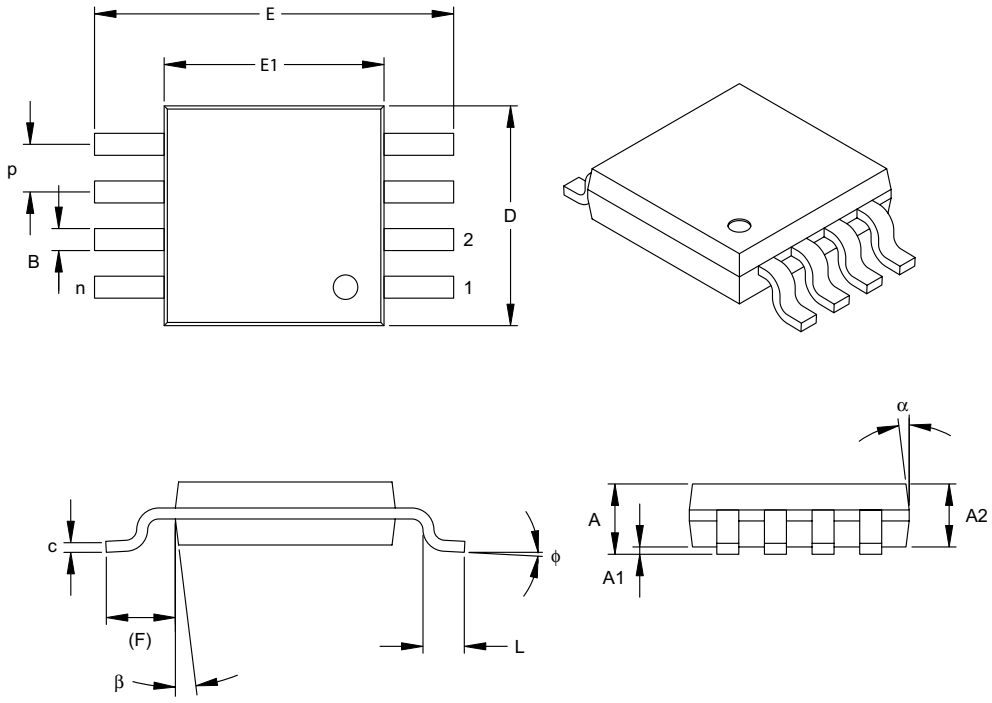
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

JEITA (formerly EIAJ) equivalent: SC-74A

Drawing No. C04-120

8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E		.193 TYP.			4.90 BSC	
Molded Package Width	E1		.118 BSC			3.00 BSC	
Overall Length	D		.118 BSC			3.00 BSC	
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F		.037 REF			0.95 REF	
Foot Angle	φ	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	α	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°	5°	-	15°

*Controlling Parameter

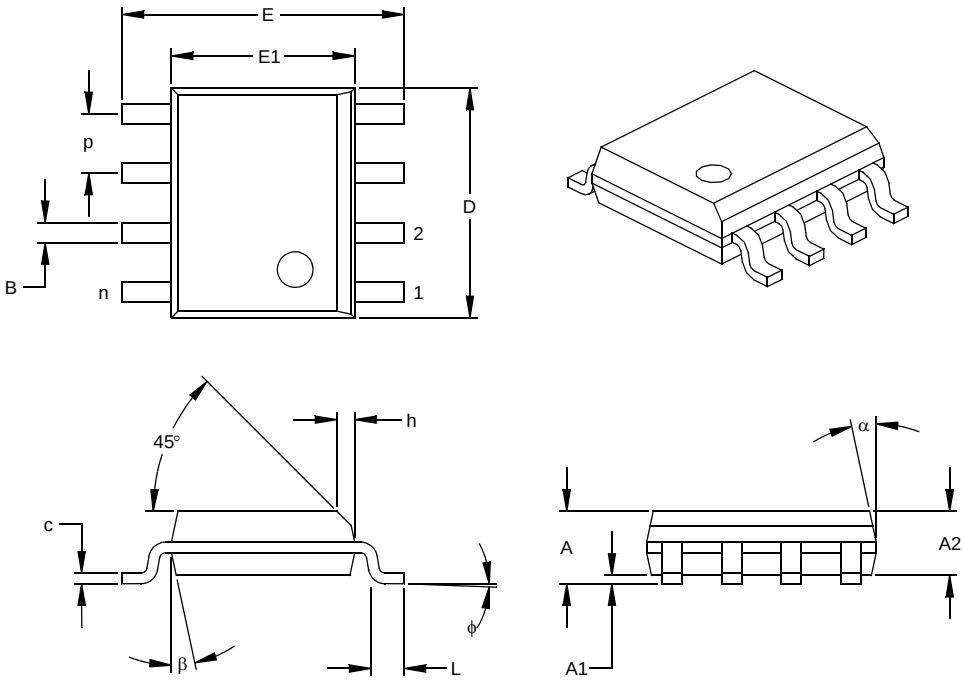
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-187

Drawing No. C04-111

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

APPENDIX A: REVISION HISTORY

Revision A (April 2005)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XXX	X	/XX
Device	Resistance Version	Temperature Range	Package

Device:	MCP4021:	Single Potentiometer with U/$\overline{D}$ Interface
	MCP4021T:	Single Potentiometer with U/$\overline{D}$ Interface (Tape and Reel) (SOIC, MSOP)
	MCP4022:	Single Rheostat with U/D interface
	MCP4022T:	Single Rheostat with U/D interface (Tape and Reel) (SOIC, MSOP)
	MCP4023:	Single Potentiometer to GND with U/$\overline{D}$ Interface
	MCP4023T:	Single Potentiometer to GND with U/$\overline{D}$ Interface (Tape and Reel) (SOIC, MSOP)
	MCP4024:	Single Rheostat to GND with U/$\overline{D}$ Interface
	MCP4024T:	Single Rheostat to GND with U/$\overline{D}$ Interface (Tape and Reel) (SOIC, MSOP)
Resistance Version:	203 = 2 kΩ	
	503 = 5 kΩ	
	104 = 10 kΩ	
	504 = 50 kΩ	
Temperature Range:	E = -40°C to +125°C	
Package:	CH = Plastic Small Outline Transistor, 6-lead	
	MS = Plastic MSOP, 8-lead	
	SN = Plastic SOIC, (150 mil Body), 8-lead	
	OT = Plastic Small Outline Transistor, 5-lead	

Examples:

a)	MCP4021-203E/SN	2 kΩ, 8-LD SOIC.
b)	MCP4021T-203E/SN	T/R, 2 kΩ, 8-LD SOIC.
c)	MCP4021-203E/MS	2 kΩ, 8-LD MSOP.
d)	MCP4021T-203E/MS	T/R, 2 kΩ, 8-LD MSOP.
e)	MCP4021-503E/SN	5 kΩ, 8-LD SOIC.
f)	MCP4021T-503E/SN	T/R, 5 kΩ, 8-LD SOIC.
g)	MCP4021-503E/MS	5 kΩ, 8-LD MSOP.
h)	MCP4021T-503E/MS	T/R, 5 kΩ, 8-LD MSOP.
i)	MCP4021-104E/SN	10 kΩ, 8-LD SOIC.
j)	MCP4021T-104E/SN	T/R, 10 kΩ, 8-LD SOIC.
k)	MCP4021-104E/MS	10 kΩ, 8-LD MSOP.
l)	MCP4021T-104E/MS	T/R, 10 kΩ, 8-LD MSOP.
m)	MCP4021-504E/SN	50 kΩ, 8-LD SOIC.
n)	MCP4021T-504E/SN	T/R, 50 kΩ, 8-LD SOIC.
o)	MCP4021-504E/MS	50 kΩ, 8-LD MSOP.
p)	MCP4021T-504E/MS	T/R, 50 kΩ, 8-LD MSOP.
a)	MCP4022T-203E/CH	2 kΩ, 6-LD SOT-23.
b)	MCP4022T-503E/CH	5 kΩ, 6-LD SOT-23.
c)	MCP4022T-104E/CH	10 kΩ, 6-LD SOT-23.
d)	MCP4022T-504E/CH	50 kΩ, 6-LD SOT-23.
a)	MCP4023T-203E/CH	2 kΩ, 6-LD SOT-23.
b)	MCP4023T-503E/CH	5 kΩ, 6-LD SOT-23.
c)	MCP4023T-104E/CH	10 kΩ, 6-LD SOT-23.
d)	MCP4023T-504E/CH	50 kΩ, 6-LD SOT-23.
a)	MCP4024T-203E/OT	2 kΩ, 5-LD SOT-23.
b)	MCP4024T-503E/OT	5 kΩ, 5-LD SOT-23.
c)	MCP4024T-104E/OT	10 kΩ, 5-LD SOT-23.
d)	MCP4024T-504E/OT	50 kΩ, 5-LD SOT-23.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona and Mountain View, California in October 2003. The Company's quality system processes and procedures are for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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