LSISAS1068 8-Port, 3 Gbit/s Serial Attached SCSI Controller

Datasheet

Version 2.0

The LSISAS1068 is an eight, port 3.0 Gbit/s SAS/SATA controller that is compliant with the Fusion-MPT™ architecture, provides a PCI-X interface, and supports Integrated RAID.

Each of the eight phys on the LSISAS1068 is capable of 3.0 Gbit/s and 1.5 Gbit/s link rates. The user can configure ports as wide or narrow. Narrow ports have one phy per port. Wide ports have between two and four phys per port. Each port supports the SSP, SMP, STP, and SATA protocols.

The SAS interface uses the proven SCSI command set to ensure reliable data transfers, while providing the connectivity and flexibility of point-to-point serial data transfers. The SAS interface provides improved performance, simplified cabling, smaller connectors, lower pin count, and lower power requirements when compared to parallel SCSI. SAS controllers leverage an electrical and physical connection interface that is compatible with Serial ATA technology. The LSISAS1068 supports the ANSI *Serial Attached SCSI* standard. Figure 1 and Figure 2 provide examples of LSISAS1068 applications.

Figure 1 LSISAS1068 Direct-Connect Example

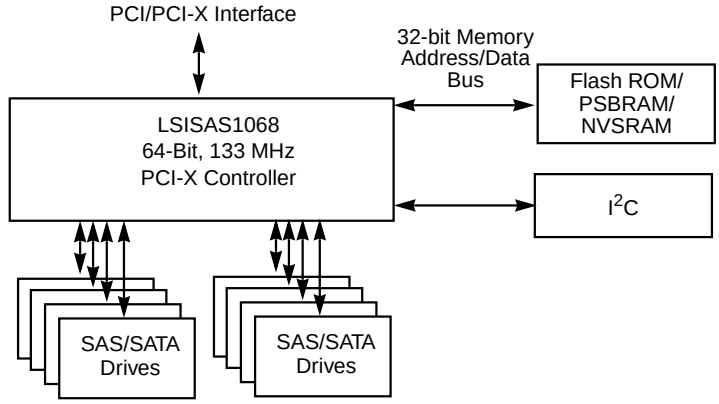
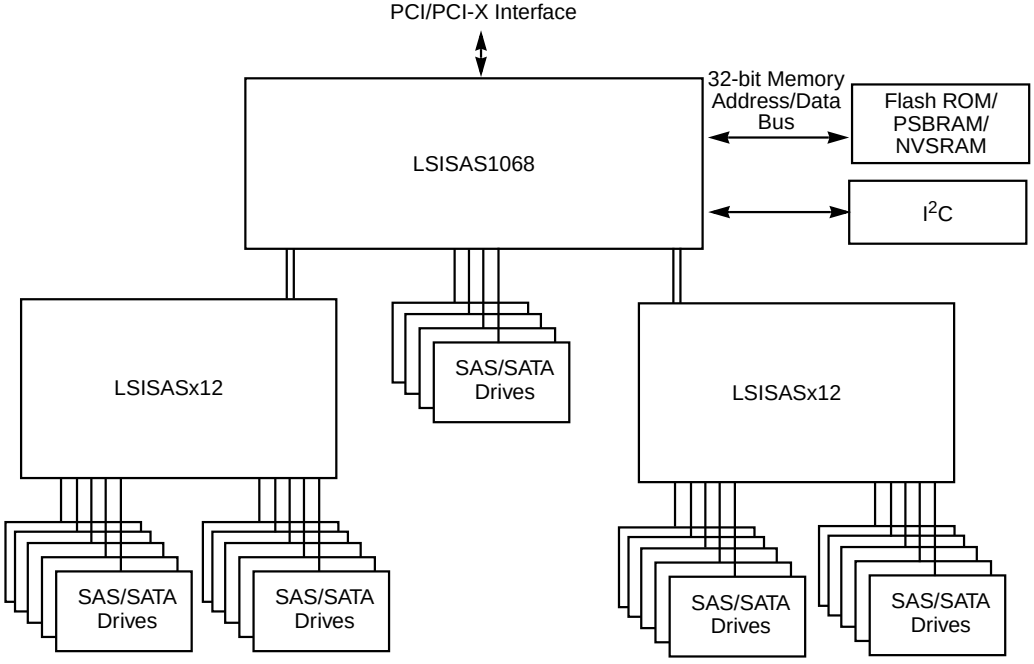


Figure 2 LSISAS1068 Controller and LSISASx12 Expander Example



The LSISAS1068 supports a 133 MHz, 64-bit PCI-X bus. With the exception that the PCI interface is not tolerant of 5V PCI, the interface is backward compatible with all revisions of the PCI/PCI-X bus. The LSISAS1068 supports PCI-X split completion cycles and 32-bit or 64-bit data bursts with variable burst length. The LSISAS1068 supports the PCI-X Addendum to the Peripheral Components Interface Specification, Revision 2.0, and the Peripheral Components Interface Specification, Revision 3.0.

The LSISAS1068 supports the Integrated RAID hardware solution, which is a highly integrated, low cost RAID solution. It is designed for systems requiring redundancy and high availability, but not needing a full-featured RAID implementation. Integrated RAID includes Integrated Mirroring™ (IM) and Integrated Striping™ (IS) technology. IM provides physical mirroring up to eight physical drives, and can perform mirroring of the boot volume through the LSISAS1068 firmware. IM requires an NVSRAM to support write journaling. IS enables data striping across up to eight physical drives. Integrated RAID is OS independent, easy to install and configure, and does not require a special driver. A single firmware build

supports all Integrated RAID capabilities. The LSISAS1068 also provides Zero Channel RAID (ZCR) support.

The LSISAS1068 uses the Fusion-MPT (Message Passing Technology) architecture, which features a performance based message passing protocol that offloads the host CPU by completely managing all I/Os and minimizes system bus overhead by coalescing interrupts. The Fusion-MPT architecture requires only thin, easy to develop device drivers that are independent of the I/O bus. LSI Logic provides these device drivers.

To meet its flexibility and data transfer requirements, the LSISAS1068 uses an ARM966 processor that operates at 225 MHz. LSI Logic manufactures the LSISAS1068 controller using Gflx™ technology.

Features

This section lists the features of the LSISAS1068.

SAS Features

This section describes the SAS features.

- Each phy supports 3.0 Gbit/s and 1.5 Gbit/s SAS data transfers
- Provides a serial, point-to-point, enterprise-level storage interface
- Supports wide transfers consisting of 2 to 4 phys
- Supports narrow ports consisting of a single phy
- Transfers data using SCSI information units
- Compatible with SATA target devices

STP/SATA Features

This section describes the STP and SATA features.

- Supports 3.0 Gbit/s and 1.5 Gbit/s SATA data transfers
- Supports STP data transfers of 3.0 Gbits/s and 1.5 Gbits/s
- Allows addressing of multiple SATA targets through an expander

- Allows multiple initiators to address a single target (in a fail-over configuration) through an expander

PCI Performance

The LSISAS1068 supports these PCI features:

- 133 MHz, 64-bit PCI/PCI-X interface that:
  - Operates up to 133 MHz PCI-X
  - Operates at 33 MHz or 66 MHz PCI
  - Supports 32-bit or 64-bit data transfers
  - Supports 32-bit or 64-bit addressing through Dual Address Cycles (DAC)
  - Provides a theoretical 1066 Mbytes/s PCI bandwidth
  - Complies with the *PCI Local Bus Specification*, Revision 3.0
  - Complies with the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 2.0
  - Complies with the *PCI Power Management Interface Specification*, Revision 1.2
  - Complies with the PC2001 Specification
- Provides unequalled performance through the Fusion-MPT architecture
- Provides high throughput and low CPU utilization to offload the host processor
- Uses a dedicated ARM966 processor
- Presents a single electrical load to the PCI Bus
- Reduces Interrupt Service Routine (ISR) overhead with interrupt coalescing
- Supports 32-bit or 64-bit data bursts with variable burst lengths
- Supports the PCI Cache Line Size register
- Supports the PCI Memory Write and Invalidate, Memory Read Line, and Memory Read Multiple commands
- Supports the PCI-X Memory Read Dword, Split Completion, Memory Read Block, Memory Write Block commands

- Supports a maximum of 16 outstanding PCI-X Split Transactions

Integration

These features make the LSISAS1068 easy to integrate:

- Supports backwards compatibility with previous revisions of the PCI specification
- Provides a full 32-bit or 64-bit PCI-X DMA bus master
- Reduces time to market with the Fusion-MPT architecture
  - Single driver binary for SAS/SATA, SCSI, and Fibre Channel products
  - One firmware build supports all Integrated RAID capabilities
  - Thin, easy to develop drivers
  - Reduced integration and certification effort

Usability

This section describes the usability features.

- Simplifies cabling with point-to-point, serial architecture
- Provides drive spin-up sequencing control
- Provides up to two LED signals for each phy to indicate drive activity and faults

Flexibility

These features increase the flexibility of the LSISAS1068:

- Supports an 8-bit Flash ROM interface, an 8-bit nonvolatile RAM (NVSRAM) interface, and a 32-bit pipelined synchronous burst SRAM (PSBRAM) interface
- Offers a flexible programming interface to tune I/O performance
- Allows mixed connections to SAS or SATA targets
- Leverages compatible connectors for SAS and Serial ATA connections
- Allows grouping of any phys within a quad port to form a wide port

- Supports Integrated RAID, which provides for Integrated Mirroring and/or Integrated Striping technology
- Provides 17 LED signals (16 of these configurable as GPIOs)
- Provides four independent GPIO signals

Reliability

These features enhance the reliability of the LSISAS1068:

- Uses proven GigaBlaze® transceivers
- Provides ESD protection
- Provides latch-up protection
- Has a high proportion of power and ground pins
- Integrated Mirroring technology provides physical mirroring of the boot volume
- Supports Zero Channel RAID

Testability

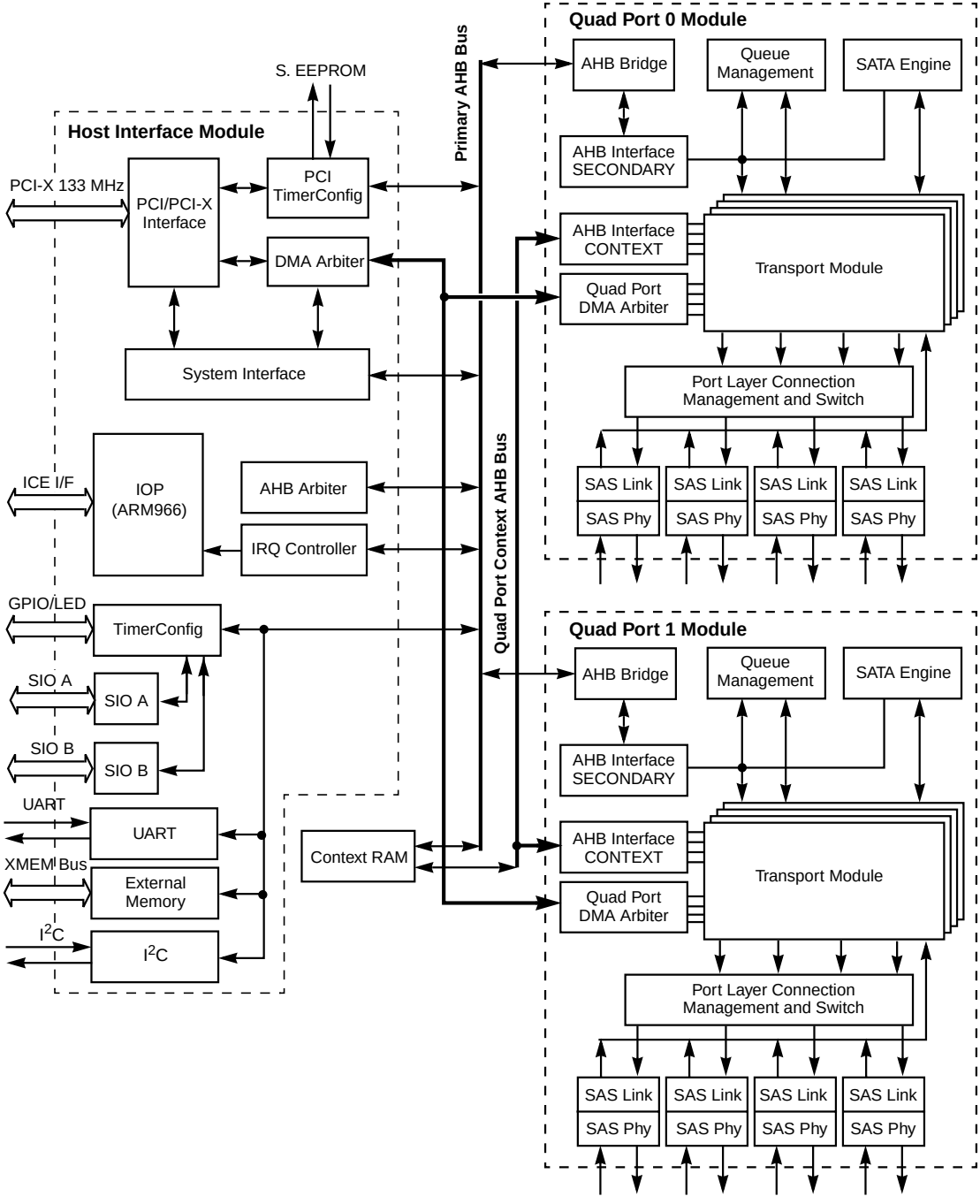
These features enhance the testability of the LSISAS1068:

- Offers JTAG boundary scan
- Offers ARM® Multi-ICE technology for debugging the ARM9 processor

Block Diagram Description

Figure 3 provides the block diagram for the LSISAS1068 controller. The following subsections discuss the block diagram. There is a single Host Interface module and 2 Quad Port modules. Each Quad Port module provides four phys.

Figure 3 LSISAS1068 Block Diagram



Host Interface Module

The LSISAS1068 interfaces with the host through the host interface module. The host interface module contains the PCI/PCI-X interface, system interface, PCI timer and configuration, DMA arbiter, IOP, I^2C, SIO A, SIO B, UART, and external memory blocks.

PCI/PCI-X Interface

The LSISAS1068 provides a PCI-X interface that supports up to a 64-bit, 133 MHz PCI-X bus. With the exception that the PCI interface is not tolerant of 5V PCI, the interface is backward compatible with all revisions of the PCI/PCI-X bus.

System Interface

In combination with the IOP, the system interface supports the Fusion-MPT architecture. The system interface efficiently passes messages between the LSISAS1068 and the host interface using a high-performance, packetized mailbox architecture. The LSISAS1068 system interface coalesces PCI interrupts to minimize traffic on the PCI bus and maximize system performance.

IOP

The LSISAS1068 I/O processor controls the system interface and manages the host side of the Fusion-MPT architecture without host processor intervention, which frees the host processor for other tasks.

Timer and Configuration

This block supports the LSISAS1068 LED and GPIO interfaces. The GPIO interface contains four independent GPIO signals. This block also supports internal timing adjustments and power-on sense configuration options.

DMA Arbiter

The LSISAS1068 provides the ability to transfer system memory blocks to and from local memory through the descriptor-based DMA arbiter and router. The DMA channel includes PCI bus master interface logic, a system DMA FIFO, and the internal bus interface logic.

PCI Timer and Configuration

This PCI Timer and Configuration module supports the PCI configuration register space, an industry-standard, 2-wire serial EEPROM interface, and a power-on reset (POR). A serial EEPROM is not required for typical system configurations.

SIO A and SIO B

The LSISAS1068 provides two serialized general purpose I/O (SGPIO) interfaces that are compliant with the SFF-8485 specification. The Serial I/O (SIO) modules provide control of the LEDs that are located in the respective Quad Port modules. SIO A controls of the LEDs in Quad Port Module 0. SIO B controls the LEDs in Quad Port Module 1.

External Memory

The external memory controller block provides an interface for Flash ROM, NVSRAM, and PSBRAM devices. The external memory bus provides a 32-bit memory bus, parity checking, and chip select signals for PSBRAM, NVSRAM, and Flash ROM. The Flash ROM and NVSRAM are capable of 8-bit accesses, while the PSBRAM is capable of 32-bit accesses.

Typical system configurations require a Flash ROM to store firmware, configuration information, and persistent data information.

I^2C

The LSISAS1068 contains an I^2C port that communicates with peripherals, such as an enclosure management processor. The I^2C port is also referred to as an Industry-Standard 2-Wire Interface (ISTWI). The I^2C block operates as either a master or a slave on the bus and sustains data rates up to 400 kbits/s. The I^2C block accomplishes byte-wise bidirectional data transfers by using either an interrupt or a polling handshake at the completion of each byte. The style and operation of this interface closely follows the defacto standard for a two-wire serial interface chip. The I^2C block controls all bus timing and performs bus-specific sequences.

UART

The UART provides test and debug access to the LSISAS1068.

Quad Port Modules 0 and 1

The Quad Port modules in the LSISAS1068 implement the SSP, SMP, and STP/SATA protocols, and manage the SAS/SATA phys. There are two Quad Port modules in the LSISASx1068. Each Quad Port module supports four phys. The following subsections describe the Quad Port modules.

Transport Module

The transport modules transmit frames to and from the port layer and implement the STP, SSP, and SMP protocols. Each Quad Port module has four instances of the transport module, one for each SAS/SATA phy on the LSISAS1068. The transport modules also manage DMA transfers.

Queue Manager

The queue manager is responsible for managing various queue structures that support the SSP, SMP, and SATA/STP protocols. The queue structures are the primary means for the IOP to initiate I/Os to the hardware, and for the hardware to notify the IOP of I/O status.

SATA Engine

The SATA engine provides information to the transport modules to enable handling of SATA commands. The SATA engine tracks queued commands per device and provides these tags to the SATA transport layer blocks.

Port Layer Connection Manager and Switch

The port layer connection monitor and switch manages transmission requests from the transport modules and originates connection requests to the SAS links. It is also responsible for handling SAS wide port configurations.

SAS Link

The SAS link layer manages SAS connections between initiator and target ports, data clocking, and CRC checking on transmitted data. The SAS link is also responsible for starting a link reset sequence.

SAS Phy

The SAS phys interface to the physical layer, perform serial-to-parallel conversion of received data and parallel-to-serial conversion of transmit data, manage phy reset sequences, and perform 8b/10b encoding.

Quad Port Arbiter

The quad port arbiter interfaces with the host interface DMA arbiter and determines bus priority between the ports for DMA transfers.

Context RAM

The context RAM is a memory that is shared between the host interface module and the quad port module. The context RAM holds a portion of the firmware.

Signal Description

The following subsections provide the signal descriptions for the LSISAS1068. A '/' following the signal indicates an active LOW signal.

PCI Signals

This section describes the PCI signals. Refer to the PCI specification for signal descriptions.

PCI System Signals

This section describes the PCI system signals.

CLK	**PCI Clock**	**Input**
RST/	**Reset**	**Input**

PCI Address and Data Signals

This section describes the PCI address and data signals.

AD[63:0]	**64-Bit Address/Data Bus**	**Input/Output**
C_BE[7:0]/	**Command/Byte Enable**	**Input/Output**

PAR	**Parity**	**Input/Output**
PAR64	**64-Bit Parity**	**Input/Output**

PCI Interface Control Signals

This section describes the PCI interface control signals.

GNT/	**Grant**	**Input**
REQ/	**Request**	**Output**
REQ64/	**Request 64-Bit**	**Input/Output**
ACK64/	**Acknowledge 64-Bit**	**Input/Output**
IDSEL	**ID Select**	**Input**
FRAME/	**Frame**	**Input/Output**
IRDY/	**Initiator Ready**	**Input/Output**
TRDY/	**Target Ready**	**Input/Output**
DEVSEL/	**Device Select**	**Input/Output**
STOP/	**Stop**	**Input/Output**
PERR/	**Parity Error**	**Input/Output**
SERR/	**Error**	**Input/Output**
INTA/	**PCI Interrupt A**	**Output**

PCI-Related Signals

ALT_INTA/ **Alternate PCI Interrupt A** **Output**
The alternate interrupt signal is used for ZCR.

ALT_GNT/ **Read/Write Chip Select** **Input**
This active LOW signal provides a chip select during configuration read and write transactions. Enabling Zero Channel RAID enables this signal.

ZCR_EN/ **Zero Channel RAID Enable** **Input**
This input configures the LSISAS1068 for ZCR operation. When ZCR_EN/ is asserted, the LSISAS1068 uses the ALT_INTA/ and ALT_GNT/ signals. Deasserting this signal configures the LSISAS1068 for standard PCI/PCI-X operation, using the INTA/ and IDSEL/ signals. This input is internally pulled HIGH.

BZR_SET **Reference Resistance** **Analog**
This signal provides the reference resistor node for the PCI-X impedance controller.

BZVDD **Reference Resistance** **Analog**
This signal provides the reference resistor node for PCI-X impedance controller.

Compact PCI Signals

This section describes the CompactPCI signals.

CPCI_EN/ **CompactPCI Enable** **Input**
Enabling this active LOW signal configures the LSISAS1068 for the CompactPCI protocol. This signal is internally pulled HIGH.

CPCI_SWITCH
CompactPCI Switch **Input**
This active HIGH signal indicates to the LSISAS1068 device that a change in the system configuration is imminent. This signal is internally pulled LOW.

CPCI_ENUM/ **CompactPCI** **Input/Output**
This signal informs the system that a board either was freshly inserted or is about to be extracted. This signal remains asserted until the system driver services the hot-swapped board.

CPCI64_EN/ **CompactPCI 64-Bit Enable** **Input**
This pin indicates the width of the PCI bus when CompactPCI is enabled. Designers must provide a pull-up on this pin when the device is enabled for Compact PCI operation. When Compact PCI is not enabled, designers must leave this pin unconnected.

CPCI_LED/ **CompactPCI LED** **Output**
This active LOW pin provides the CompactPCI Status LED. This is a 3.3 V output.

SAS Signals

This section describes the SAS interface signals.

REFCLK_P, REFCLK_N **Input**
These pins provide the serial differential clock. Connect a 75 MHz oscillator with an accuracy of at least ± 50 ppm to these pins. To use a single-ended crystal, tie the crystal to REFCLK_P and tie REFCLK_N to a resistor termination.

RTRIM **Resistor Reference** **Analog**
This pin provides the analog resistor reference for the GigaBlaze transceivers.

RX[7:0]– **Receive Negative Differential Data** **Input**
RX[x]– provides the negative differential data receiver for phy[x].

RX[7:0]+ **Receive Positive Differential Data** **Input**
RX[x]+ provides the positive differential data receiver for phy[x].

TX[7:0]– **Transmit Negative Differential Data** **Output**
TX[x]– provides the negative differential data transmit signal for phy[x].

TX[7:0]+ **Transmit Positive Differential Data** **Output**
TX[x]+ provides the positive differential data transmit signal for each phy[x].

I^2C and Serial EEPROM Signals

This section describes the serial EEPROM and I^2C signals.

SERIAL_CLK **Serial Interface Clock** **Input/Output**
This pin provides the serial EEPROM clock signal. This pin is internally pulled HIGH.

SERIAL_DATA **Serial Interface Data** **Input/Output**
This pin provides the serial EEPROM data signal. This pin is internally pulled HIGH.

ISTWI_CLK	**I^2C Clock**	**Input/Output**
	This pin provides the I^2C clock signal.	
ISTWI_DATA	**I^2C Data**	**Input/Output**
	This pin provides the I^2C data signal.	

Memory Interface Signals

This section describes the memory interface pins.

MCLK	**Memory Clock**	**Output**
	All synchronous RAM control/data signals reference the rising edge of this clock.	
ADSC/	**Address-Strobe-Controller**	**Output**
	Asserting this active LOW signal initiates READ, WRITE, or chip deselect cycles.	
ADV/	**Advance**	**Output**
	Asserting this active LOW signal increments the burst address counter of the selected synchronous SRAM.	
MAD[31:0]	**Multiplexed Address/Data**	**Input/Output**
	These signals provide the address and data bus to the PSBRAM, Flash ROM, and NVSRAM. These signals also provide Power-On Sense configuration functions to the LSISAS1068. These signals are internally pulled LOW.	

Important: Provide pull-up resistors for these pins.

MADP[3:0]	**Memory Parity**	**Input/Output**
	These signals provide parity checking for MAD[31:0]. These signals are internally pulled HIGH.	
MOE[1:0]/	**Memory Output Enables**	**Output**
	Asserting these active LOW signals enable the selected PSBRAM, Flash ROM, or NVSRAM device to drive data. MOE[1]/ enables PSBRAM and Flash ROM devices. MOE[0]/ enables NVSRAM devices. MOE[1:0]/ allow interleaved PSBRAM configurations.	
MWE[1:0]/	**Memory Write Enables**	**Output**
	The LSISAS1068 uses these active LOW bank write signals for interleaved PSBRAM configurations.	

BWE[3:0]/ **Memory Byte Write Enables** **Output**
Asserting these active LOW, byte-lane write signals enable partial word writes to the PSBRAM. BWE[3]/ and BWE[2]/ enable partial word writes to the Flash ROM and the NVSRAM if FLASH_CS/ or NVSRAM_CS/ are asserted.

NVSRAM_CS/ **NVSRAM Chip Select** **Output**
Asserting this active LOW signal selects the NVSRAM device.

PSBRAM_CS/ **RAM Chip Select** **Output**
Asserting this active LOW signal selects the PSBRAMs. Up to four PSBRAMS are possible in an interleaved and depth-expanded configuration.

FLASH_CS/ **Flash Chip Select** **Output**
Asserting the active LOW signal selects the Flash ROM. The LSISAS1068 maps Flash ROM address space into system memory space.

SIO Pins

This section describes the SIO A and SIO B pins.

SIO_CLK_A **SIO Clock** **Output**
This signal provides the clock signal for SIO A.

SIO_CLK_B **SIO Clock** **Output**
This signal provides the clock signal for SIO B.

SIO_DIN_A **SIO Data In A** **Input**
This pin provides the data input signal to the SIO interface for Quad Port 0.

SIO_DIN_B **SIO Data In B** **Input**
This pin provides the data input signal to the SIO interface for Quad Port 1.

SIO_DOUT_A **SIO Data Out A** **Output**
This signal provides the data output signal to the SIO bus from Quad Port 0. This signal controls the Quad Port 0 LED drives.

SIO_DOUT_B **SIO Data Out B** **Output**
This signal provides the data output signal to the SIO bus from Quad Port 1. This signal controls the Quad Port 1 LED drives.

SIO_END_A **SIO End Control** **Output**
The SIO module drives this output to end control of the SIO bus on Quad Port 0.

SIO_END_B **SIO End Control** **Output**
The SIO module drives this output to end control of the SIO bus on Quad Port 1.

Configuration and General Purpose Signals

This section describes the configuration and general purpose pins.

TST_RST/ **Test Reset** **Input**
Asserting this signal forces the chip into a Power-On-Reset (POR) state. This signal has an internal pull-up.

REFCLK_B **ARM Reference Clock** **Input**
This pin provides the ARM reference clock. This pin has an internal pull-down.

Note: See the reference schematics provided by the LSI Logic SSP Systems Engineering group, for details regarding how to connect REFCLK_B to the REFCLK_P and REFCLK_N network.

MODE[5:0] **Mode Select** **Input**
This 6-bit bus defines operational and test modes for the chip. These pins have internal pull-downs.

FAULT_LED[7:0]/
Fault LED **Output**
These output signals indicate a SAS link fault.

ACTIVE_LED[7:0]/
Activity LED **Output**
These output signals indicate SAS link activity.

GPIO[3:0] **General Purpose I/O** **Input/Output**
These pins provide general purpose input/output signals. These pins have internal pull-ups.

HB_LED/	**Heartbeat LED** Firmware intermittently asserts this signal to indicate that the IOP is operational.	**Output**

JTAG and Test Signals

This section describes the test and JTAG signals.

FSELA	**Clock Select** LSI Logic factory test only. Pull this signal LOW.	**Input**
TCK	**JTAG Debug Clock**	**Input**
TRST/	**JTAG Debug Reset**	**Input**
TDI	**JTAG Debug Test Data In**	**Input**
TDO	**JTAG Debug Test Data Out**	**Output**
TMS	**JTAG Debug Test Mode Select**	**Input**
TCK_ICE	**Multi-ICE Debug Clock**	**Input**
RTCK_ICE	**Multi-ICE Debug Return Clock**	**Output**
TRST_ICE/	**Multi-ICE Debug Reset**	**Input**
TDI_ICE	**Multi-ICE Debug Test Data In**	**Input**
TDO_ICE	**Multi-ICE Debug Test Data Out**	**Output**
TMS_ICE	**Multi-ICE Debug Test Mode Select**	**Input**
IDDTN	**IDDQ Test Mode Enable** LSI Logic factory test only. Pull this signal LOW.	**Input**
TN/	**3-State Output Enable Control** LSI Logic factory test only. Pull this signal HIGH.	**Input**
PROCMON	**Process Monitor Test Output Driver** LSI Logic factory test only.	**Output**
SCAN_ENABLE	**Test Input Pin** LSI Logic factory test only. Pull this signal LOW.	**Input**
SCAN_MODE	**Test Input Pin** LSI Logic factory test only. Pull this signal LOW.	**Input**

ECC[5:2]	**Test Pins** LSI Logic factory test only.	**Input/Output**
SPARE[3:2]	**Test Mux Spare** LSI Logic factory test only.	**Input/Output**
TDIODE_P	**Anode Connection of the Thermal Diode**	**Input**
TDIODE_N	**Cathode Connection of the Thermal Diode**	**Output**
UART_RX	**UART Receive**	**Input**
UART_TX	**UART Transmit**	**Output**
RESERVED	**Reserved** LSI Logic factory test only. These signals must be left unconnected.	**Input**

Power Signals

This section describes the power and ground signals.

REFPLL_VDD **Power**
These signals provide 1.2 V power.

REFPLL_VSS **Ground**
These signals provide ground.

PLL_VDD **Power**
These signals provide 1.2 V power.

PLL_VSS **Ground**
These signals provide ground.

VDD2 **Power**
These signals provide 1.2 V core power.

VDDIO33 **Power**
These signals provide 3.3 V I/O power.

VSS2 **Ground**
These signals provide ground.

RX_VSS[7:0], RXB_VSS[7:0], TX_VSS[7:0], TXB_VSS[7:0] **Ground**
These signals provide ground for the GigaBlaze core.

RX_VDD[7:0], RXB_VDD[7:0], TX_VDD[7:0], TXB_VDD[7:0] **Power**
These signals provide 1.2 V power for the GigaBlaze core.

Pin Listing

Table 1 and Table 2 provide pin listings for the LSISAS1068. Figure 4 provide the BGA diagram.

Table 1 Listing by Signal Name[1]

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
ACK64/	AC16	AD[51]	AD24	IDDT	V2	N/C	J2
ACTIVE_LED[0]/	H3	AD[52]	AA19	INTA/	Y1	N/C	J5
ACTIVE_LED[1]/	F1	AD[53]	AD23	IRDY/	AF8	N/C	J21
ACTIVE_LED[2]/	H4	AD[54]	AF23	ISTWI_CLK	H23	N/C	J26
ACTIVE_LED[3]/	H6	AD[55]	AE24	ISTWI_DATA	D24	N/C	K5
ACTIVE_LED[4]/	J6	AD[56]	AF22	MAD[0]	E26	N/C	K6
ACTIVE_LED[5]/	J4	AD[57]	AE23	MAD[1]	F26	N/C	K21
ACTIVE_LED[6]/	J3	AD[58]	AE22	MAD[2]	K22	N/C	L5
ACTIVE_LED[7]/	G1	AD[59]	AC20	MAD[3]	D25	N/C	L6
AD[0]	AC14	AD[60]	AD19	MAD[4]	G23	N/C	L21
AD[1]	AB16	AD[61]	AB18	MAD[5]	J24	N/C	L22
AD[2]	AB14	AD[62]	AF20	MAD[6]	J23	N/C	M22
AD[3]	AD14	AD[63]	AC18	MAD[7]	E25	N/C	N1
AD[4]	AF14	ADSC/	R21	MAD[8]	G26	N/C	N21
AD[5]	AC15	ADV/	R23	MAD[9]	K23	N/C	N25
AD[6]	AB13	ALT_INTA/	U5	MAD[10]	H24	N/C	P6
AD[7]	AE13	ALT_GNT/	AA1	MAD[11]	D26	N/C	P21
AD[8]	AF12	BZR_SET	V21	MAD[12]	H25	N/C	R5
AD[9]	AD13	BZVDD	AA26	MAD[13]	J25	N/C	R22
AD[10]	AF9	BWE[0]/	P22	MAD[14]	M21	N/C	T5
AD[11]	AA12	BWE[1]/	P25	MAD[15]	K25	N/C	U21
AD[12]	AF10	BWE[2]/	L26	MAD[16]	U25	N/C	U22
AD[13]	AF11	BWE[3]/	P26	MAD[17]	T26	N/C	V22
AD[14]	AE10	C_BE[0]/	AC12	MAD[18]	U26	N/C	W2
AD[15]	AE8	C_BE[1]/	AA11	MAD[19]	R26	N/C	W6
AD[16]	AC8	C_BE[2]/	AC9	MAD[20]	V26	N/C	Y5
AD[17]	AD8	C_BE[3]/	AA6	MAD[21]	T22	N/C	Y7
AD[18]	AB7	C_BE[4]/	AB15	MAD[22]	W25	N/C	Y21
AD[19]	AF4	C_BE[5]/	AC17	MAD[23]	V25	N/C	AA7
AD[20]	AB6	C_BE[6]/	AE17	MAD[24]	T23	N/C	AA8
AD[21]	AD5	C_BE[7]/	AF19	MAD[25]	V24	N/C	AA9
AD[22]	AA4	CLK	Y6	MAD[26]	U24	N/C	AA13
AD[23]	AC7	CPCI64_EN/	U6	MAD[27]	U23	N/C	AA14
AD[24]	AE4	CPCI_EN/	T6	MAD[28]	W26	N/C	AA15
AD[25]	AC5	CPCI_LED/	N6	MAD[29]	T21	N/C	AA17
AD[26]	AB5	CPCI_ENUM/	U4	MAD[30]	W24	N/C	AA18
AD[27]	AE2	CPCI_SWITCH	U3	MAD[31]	V23	N/C	AA21
AD[28]	AC3	DEVSEL/	AF6	MCLK	P23	N/C	AB3
AD[29]	AB4	ECC2	AC1	MODE[0]	E2	N/C	AB8
AD[30]	V6	ECC3	W4	MODE[1]	D1	N/C	AB10
AD[31]	AC4	ECC4	AB1	MODE[2]	G4	N/C	AB11
AD[32]	AB25	ECC5	V5	MODE[3]	D2	N/C	AB12
AD[33]	AC26	FAULT_LED[0]/	K3	MODE[4]	F4	N/C	AB17
AD[34]	W22	FAULT_LED[1]/	K4	MODE[5]	G6	N/C	AB19
AD[35]	Y23	FAULT_LED[2]/	H1	MOE0/	M26	N/C	AB23
AD[36]	W21	FAULT_LED[3]/	H2	MOE1/	H26	N/C	AB26
AD[37]	AC24	FAULT_LED[4]/	L4	MADP[0]	J22	N/C	AC13
AD[38]	W23	FAULT_LED[5]/	J1	MADP[1]	N24	N/C	AD4
AD[39]	Y22	FAULT_LED[6]/	K1	MADP[2]	P24	N/C	AD9
AD[40]	AC25	FAULT_LED[7]/	K2	MADP[3]	Y26	N/C	AD18
AD[41]	AD25	FLASH_CS/	L23	MWE0/	N26	N/C	AE9
AD[42]	AC23	FRAME/	AB9	MWE1/	K26	N/C	AE14
AD[43]	AC22	FSELA	E3	N/C	C2	N/C	AE18
AD[44]	Y20	GNT/	AC2	N/C	C25	N/C	AE25
AD[45]	AD22	GPIO[0]	P5	N/C	D3	N/C	AF15
AD[46]	AA20	GPIO[1]	P4	N/C	D23	N/C	AF17
AD[47]	AA23	GPIO[2]	R1	N/C	E1	N/C	AF18
AD[48]	AB21	GPIO[3]	P3	N/C	E24		
AD[49]	AC21	HB_LED/	M5	N/C	G5		
AD[50]	AA22	IDSEL	AE3	N/C	H5		

1. Pad locations marked N/C are not internally connected to the LSISAS1068 silicon. Pad locations marked RESERVED are for LSI Logic factory test use only. Refer to the Signal Description section to determine how to terminate the RESERVED pads.

Table 1 Listing by Signal Name (Cont.)[1]

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
N/C	AF21	RXB_VDD5	C10	TX_VDD0	A23	VDD2	T11
NVSRAM_CS/	K24	RXB_VDD6	E9	TX_VDD1	D18	VDD2	T13
PAR	AC11	RXB_VDD7	G8	TX_VDD2	C17	VDD2	T15
PAR64	AE19	RXB_VSS0	F21	TX_VDD3	D14	VDD2	T17
PBSRAM_CS/	M23	RXB_VSS1	F19	TX_VDD4	D10	VDD2	U10
PERR/	AA10	RXB_VSS2	E17	TX_VDD5	D8	VDD2	U12
PLLVDD	AD3	RXB_VSS3	G16	TX_VDD6	C4	VDD2	U14
PLLVSS	AA5	RXB_VSS4	F13	TX_VDD7	E5	VDD2	U16
PROCMON	U2	RXB_VSS5	F11	TX_VSS0	E19	VDDIO33	A24
REFCLK_B	B13	RXB_VSS6	G10	TX_VSS1	G18	VDDIO33	B2
REFCLK_N	D12	RXB_VSS7	C7	TX_VSS2	D16	VDDIO33	B11
REFCLK_P	C13	SCAN_ENABLE	E4	TX_VSS3	E14	VDDIO33	B12
REFPLL_VDD	B14	SCAN_MODE	F5	TX_VSS4	E11	VDDIO33	B15
REFPLL_VSS	A13	SERIAL_CLK	F23	TX_VSS5	A7	VDDIO33	B16
REQ/	Y4	SERIAL_DATA	H21	TX_VSS6	F8	VDDIO33	C1
REQ64/	AD17	SERR/	AE5	TX_VSS7	F7	VDDIO33	C5
RESERVED	V4	SIO_CLK_A	F22	TXB_VDD0	F20	VDDIO33	C6
RESERVED	W3	SIO_CLK_B	M4	TXB_VDD1	E18	VDDIO33	C20
RST/	W5	SIO_DIN_A	G21	TXB_VDD2	F16	VDDIO33	C21
RTCK_ICE	N3	SIO_DIN_B	M1	TXB_VDD3	A14	VDDIO33	C26
RTRIM	C14	SIO_DOUT_A	G22	TXB_VDD4	F12	VDDIO33	D13
RX0+	B24	SIO_DOUT_B	M6	TXB_VDD5	E10	VDDIO33	F2
RX0–	B25	SIO_END_A	C24	TXB_VDD6	C8	VDDIO33	F25
RX1+	B20	SIO_END_B	L1	TXB_VDD7	G7	VDDIO33	G2
RX1–	B21	SPARE2	G20	TXB_VSS0	E20	VDDIO33	G9
RX2+	A19	SPARE3	E22	TXB_VSS1	B19	VDDIO33	G11
RX2–	A20	STOP/	AF7	TXB_VSS2	E16	VDDIO33	G12
RX3+	A17	TCK	T1	TXB_VSS3	F14	VDDIO33	G13
RX3–	B17	TCK_ICE	N5	TXB_VSS4	D11	VDDIO33	G14
RX4+	A10	TDI	R6	TXB_VSS5	F10	VDDIO33	G15
RX4–	A11	TDI_ICE	P2	TXB_VSS6	E8	VDDIO33	G17
RX5+	B8	TDIODE_P	N22	TXB_VSS7	D4	VDDIO33	G19
RX5–	A8	TDIODE_VSS	N23	UART_RX	E23	VDDIO33	G25
RX6+	B6	TDO	R4	UART_TX	H22	VDDIO33	H7
RX6–	B7	TDO_ICE	P1	VDD2	K11	VDDIO33	H20
RX7+	B3	TMS	V1	VDD2	K13	VDDIO33	J7
RX7–	C3	TMS_ICE	N2	VDD2	K15	VDDIO33	J20
RX_VDD0	E21	TN/	T4	VDD2	K17	VDDIO33	K7
RX_VDD1	D19	TRDY/	AC10	VDD2	L10	VDDIO33	K20
RX_VDD2	C18	TRST/	U1	VDD2	L12	VDDIO33	L2
RX_VDD3	D15	TRST_ICE/	N4	VDD2	L14	VDDIO33	L7
RX_VDD4	B10	TST_RST/	F6	VDD2	L16	VDDIO33	L20
RX_VDD5	D9	TX0+	B22	VDD2	M11	VDDIO33	L25
RX_VDD6	D7	TX0–	B23	VDD2	M13	VDDIO33	M2
RX_VDD7	E6	TX1+	A22	VDD2	M15	VDDIO33	M7
RX_VSS0	D22	TX1–	A21	VDD2	M17	VDDIO33	M20
RX_VSS1	F18	TX2+	B18	VDD2	N10	VDDIO33	M25
RX_VSS2	D17	TX2–	A18	VDD2	N12	VDDIO33	N7
RX_VSS3	F15	TX3+	A16	VDD2	N14	VDDIO33	N20
RX_VSS4	E12	TX3–	A15	VDD2	N16	VDDIO33	P7
RX_VSS5	C9	TX4+	A9	VDD2	P11	VDDIO33	P20
RX_VSS6	F9	TX4–	B9	VDD2	P13	VDDIO33	R2
RX_VSS7	E7	TX5+	A6	VDD2	P15	VDDIO33	R7
RXB_VDD0	C23	TX5–	A5	VDD2	P17	VDDIO33	R20
RXB_VDD1	C19	TX6+	B4	VDD2	R10	VDDIO33	R25
RXB_VDD2	F17	TX6–	B5	VDD2	R12	VDDIO33	T2
RXB_VDD3	E15	TX7+	A4	VDD2	R14	VDDIO33	T7
RXB_VDD4	A12	TX7–	A3	VDD2	R16	VDDIO33	T20

1. Pad locations marked N/C are not internally connected to the LSISAS1068 silicon. Pad locations marked RESERVED are for LSI Logic factory test use only. Refer to the Signal Description section to determine how to terminate the RESERVED pads.

Table 1 Listing by Signal Name (Cont.)[1]

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
VDDIO33	T25	VDDIO33	AE21	VSS	K16	VSS	T14
VDDIO33	U7	VDDIO33	AF3	VSS	K19	VSS	T16
VDDIO33	U20	VDDIO33	AF5	VSS	L3	VSS	T19
VDDIO33	V3	VDDIO33	AF13	VSS	L8	VSS	T24
VDDIO33	V7	VDDIO33	AF16	VSS	L11	VSS	U8
VDDIO33	V20	VDDIO33	AF24	VSS	L13	VSS	U11
VDDIO33	W7	VSS	A2	VSS	L15	VSS	U13
VDDIO33	W20	VSS	A25	VSS	L17	VSS	U15
VDDIO33	Y2	VSS	B1	VSS	L19	VSS	U17
VDDIO33	Y8	VSS	B26	VSS	L24	VSS	U19
VDDIO33	Y9	VSS	C11	VSS	M3	VSS	V8
VDDIO33	Y10	VSS	C12	VSS	M8	VSS	V19
VDDIO33	Y11	VSS	C15	VSS	M10	VSS	W8
VDDIO33	Y12	VSS	C16	VSS	M12	VSS	W9
VDDIO33	Y13	VSS	C22	VSS	M14	VSS	W10
VDDIO33	Y14	VSS	D5	VSS	M16	VSS	W11
VDDIO33	Y15	VSS	D6	VSS	M19	VSS	W12
VDDIO33	Y16	VSS	D20	VSS	M24	VSS	W13
VDDIO33	Y17	VSS	D21	VSS	N8	VSS	W14
VDDIO33	Y18	VSS	E13	VSS	N11	VSS	W15
VDDIO33	Y19	VSS	F3	VSS	N13	VSS	W16
VDDIO33	Y25	VSS	F24	VSS	N15	VSS	W17
VDDIO33	AA2	VSS	G3	VSS	N17	VSS	W18
VDDIO33	AA16	VSS	G24	VSS	N19	VSS	W19
VDDIO33	AA25	VSS	H8	VSS	P8	VSS	Y3
VDDIO33	AB2	VSS	H9	VSS	P10	VSS	Y24
VDDIO33	AB20	VSS	H10	VSS	P12	VSS	AA3
VDDIO33	AB22	VSS	H11	VSS	P14	VSS	AA24
VDDIO33	AB24	VSS	H12	VSS	P16	VSS	AD6
VDDIO33	AC6	VSS	H13	VSS	P19	VSS	AD7
VDDIO33	AC19	VSS	H14	VSS	R3	VSS	AD11
VDDIO33	AD1	VSS	H15	VSS	R8	VSS	AD12
VDDIO33	AD2	VSS	H16	VSS	R11	VSS	AD15
VDDIO33	AD10	VSS	H17	VSS	R13	VSS	AD16
VDDIO33	AD26	VSS	H18	VSS	R15	VSS	AD20
VDDIO33	AE6	VSS	H19	VSS	R17	VSS	AD21
VDDIO33	AE7	VSS	J8	VSS	R19	VSS	AE1
VDDIO33	AE11	VSS	J19	VSS	R24	VSS	AE26
VDDIO33	AE12	VSS	K8	VSS	T3	VSS	AF2
VDDIO33	AE15	VSS	K10	VSS	T8	VSS	AF25
VDDIO33	AE16	VSS	K12	VSS	T10	ZCR_EN/	W1
VDDIO33	AE20	VSS	K14	VSS	T12		

1. Pad locations marked N/C are not internally connected to the LSISAS1068 silicon. Pad locations marked RESERVED are for LSI Logic factory test use only. Refer to the Signal Description section to determine how to terminate the RESERVED pads.

Table 2 Listing by Pin Number[1]

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
A2	VSS	C12	VSS	E21	RX_VDD0	H4	ACTIVE_LED[2]/
A3	TX7–	C13	REFCLK_P	E22	SPARE3	H5	N/C
A4	TX7+	C14	RTRIM	E23	UART_RX	H6	ACTIVE_LED[3]/
A5	TX5–	C15	VSS	E24	N/C	H7	VDDIO33
A6	TX5+	C16	VSS	E25	MAD[7]	H8	VSS
A7	TX_VSS5	C17	TX_VDD2	E26	MAD[0]	H9	VSS
A8	RX5–	C18	RX_VDD2	F1	ACTIVE_LED[1]/	H10	VSS
A9	TX4+	C19	RXB_VDD1	F2	VDDIO33	H11	VSS
A10	RX4+	C20	VDDIO33	F3	VSS	H12	VSS
A11	RX4–	C21	VDDIO33	F4	MODE[4]	H13	VSS
A12	RXB_VDD4	C22	VSS	F5	SCAN_MODE	H14	VSS
A13	REFPLL_VSS	C23	RXB_VDD0	F6	TST_RST/	H15	VSS
A14	TXB_VDD3	C24	SIO_END_A	F7	TX_VSS7	H16	VSS
A15	TX3–	C25	N/C	F8	TX_VSS6	H17	VSS
A16	TX3+	C26	VDDIO33	F9	RX_VSS6	H18	VSS
A17	RX3+	D1	MODE[1]	F10	TXB_VSS5	H19	VSS
A18	TX2–	D2	MODE[3]	F11	RXB_VSS5	H20	VDDIO33
A19	RX2+	D3	N/C	F12	TXB_VDD4	H21	SERIAL_DATA
A20	RX2–	D4	TXB_VSS7	F13	RXB_VSS4	H22	UART_TX
A21	TX1–	D5	VSS	F14	TXB_VSS3	H23	ISTWI_CLK
A22	TX1+	D6	VSS	F15	RX_VSS3	H24	MAD[10]
A23	TX_VDD0	D7	RX_VDD6	F16	TXB_VDD2	H25	MAD[12]
A24	VDDIO33	D8	TX_VDD5	F17	RXB_VDD2	H26	MOE1/
A25	VSS	D9	RX_VDD5	F18	RX_VSS1	J1	FAULT_LED[5]/
B1	VSS	D10	TX_VDD4	F19	RXB_VSS1	J2	N/C
B2	VDDIO33	D11	TXB_VSS4	F20	TXB_VDD0	J3	ACTIVE_LED[6]/
B3	RX7+	D12	REFCLK_N	F21	RXB_VSS0	J4	ACTIVE_LED[5]/
B4	TX6+	D13	VDDIO33	F22	SIO_CLK_A	J5	N/C
B5	TX6–	D14	TX_VDD3	F23	SERIAL_CLK	J6	ACTIVE_LED[4]/
B6	RX6+	D15	RX_VDD3	F24	VSS	J7	VDDIO33
B7	RX6–	D16	TX_VSS2	F25	VDDIO33	J8	VSS
B8	RX5+	D17	RX_VSS2	F26	MAD[1]	J19	VSS
B9	TX4–	D18	TX_VDD1	G1	ACTIVE_LED[7]/	J20	VDDIO33
B10	RX_VDD4	D19	RX_VDD1	G2	VDDIO33	J21	N/C
B11	VDDIO33	D20	VSS	G3	VSS	J22	MADP[0]
B12	VDDIO33	D21	VSS	G4	MODE[2]	J23	MAD[6]
B13	REFCLK_B	D22	RX_VSS0	G5	N/C	J24	MAD[5]
B14	REFPLL_VDD	D23	N/C	G6	MODE[5]	J25	MAD[13]
B15	VDDIO33	D24	ISTWI_DATA	G7	TXB_VDD7	J26	N/C
B16	VDDIO33	D25	MAD[3]	G8	RXB_VDD7	K1	FAULT_LED[6]/
B17	RX3–	D26	MAD[11]	G9	VDDIO33	K2	FAULT_LED[7]/
B18	TX2+	E1	N/C	G10	RXB_VSS6	K3	FAULT_LED[0]/
B19	TXB_VSS1	E2	MODE[0]	G11	VDDIO33	K4	FAULT_LED[1]/
B20	RX1+	E3	FSELA	G12	VDDIO33	K5	N/C
B21	RX1–	E4	SCAN_ENABLE	G13	VDDIO33	K6	N/C
B22	TX0+	E5	TX_VDD7	G14	VDDIO33	K7	VDDIO33
B23	TX0–	E6	RX_VDD7	G15	VDDIO33	K8	VSS
B24	RX0+	E7	RX_VSS7	G16	RXB_VSS3	K10	VSS
B25	RX0–	E8	TXB_VSS6	G17	VDDIO33	K11	VDD2
B26	VSS	E9	RXB_VDD6	G18	TX_VSS1	K12	VSS
C1	VDDIO33	E10	TXB_VDD5	G19	VDDIO33	K13	VDD2
C2	N/C	E11	TX_VSS4	G20	SPARE2	K14	VSS
C3	RX7–	E12	RX_VSS4	G21	SIO_DIN_A	K15	VDD2
C4	TXVDD6	E13	VSS	G22	SIO_DOUT_A	K16	VSS
C5	VDDIO33	E14	TX_VSS3	G23	MAD[4]	K17	VDD2
C6	VDDIO33	E15	RXB_VDD3	G24	VSS	K19	VSS
C7	RXB_VSS7	E16	TXB_VSS2	G25	VDDIO33	K20	VDDIO33
C8	TXB_VDD6	E17	RXB_VSS2	G26	MAD[8]	K21	N/C
C9	RX_VSS5	E18	TXB_VDD1	H1	FAULT_LED[2]/	K22	MAD[2]
C10	RXB_VDD5	E19	TX_VSS0	H2	FAULT_LED[3]/	K23	MAD[9]
C11	VSS	E20	TXB_VSS0	H3	ACTIVE_LED[0]/	K24	NVSRAM_CS/

1. Pad locations marked N/C are not internally connected to the LSISAS1068 silicon. Pad locations marked RESERVED are for LSI Logic factory test use only. Refer to the Signal Description section to determine how to terminate the RESERVED pads.

Table 2 Listing by Pin Number (Cont.)[1]

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
K25	MAD[15]	N8	VSS	R19	VSS	V2	IDDT
K26	MWE1/	N10	VDD2	R20	VDDIO33	V3	VDDIO33
L1	SIO_END_B	N11	VSS	R21	ADSC/	V4	RESERVED
L2	VDDIO33	N12	VDD2	R22	N/C	V5	ECC5
L3	VSS	N13	VSS	R23	ADV/	V6	AD[30]
L4	FAULT_LED[4]/	N14	VDD2	R24	VSS	V7	VDDIO33
L5	N/C	N15	VSS	R25	VDDIO33	V8	VSS
L6	N/C	N16	VDD2	R26	MAD[19]	V19	VSS
L7	VDDIO33	N17	VSS	T1	TCK	V20	VDDIO33
L8	VSS	N19	VSS	T2	VDDIO33	V21	BZR_SET
L10	VDD2	N20	VDDIO33	T3	VSS	V22	N/C
L11	VSS	N21	N/C	T4	TN/	V23	MAD[31]
L12	VDD2	N22	TDIODE_P	T5	N/C	V24	MAD[25]
L13	VSS	N23	TDIODE_VSS	T6	CPCI_EN/	V25	MAD[23]
L14	VDD2	N24	MADP[1]	T7	VDDIO33	V26	MAD[20]
L15	VSS	N25	N/C	T8	VSS	W1	ZCR_EN/
L16	VDD2	N26	MWE0/	T10	VSS	W2	N/C
L17	VSS	P1	TDO_ICE	T11	VDD2	W3	RESERVED
L19	VSS	P2	TDI_ICE	T12	VSS	W4	ECC3
L20	VDDIO33	P3	GPIO[3]	T13	VDD2	W5	RST/
L21	N/C	P4	GPIO[1]	T14	VSS	W6	N/C
L22	N/C	P5	GPIO[0]	T15	VDD2	W7	VDDIO33
L23	FLASH_CS/	P6	N/C	T16	VSS	W8	VSS
L24	VSS	P7	VDDIO33	T17	VDD2	W9	VSS
L25	VDDIO33	P8	VSS	T19	VSS	W10	VSS
L26	BWE[2]/	P10	VSS	T20	VDDIO33	W11	VSS
M1	SIO_DIN_B	P11	VDD2	T21	MAD[29]	W12	VSS
M2	VDDIO33	P12	VSS	T22	MAD[21]	W13	VSS
M3	VSS	P13	VDD2	T23	MAD[24]	W14	VSS
M4	SIO_CLK_B	P14	VSS	T24	VSS	W15	VSS
M5	HB_LED/	P15	VDD2	T25	VDDIO33	W16	VSS
M6	SIO_DOUT_B	P16	VSS	T26	MAD[17]	W17	VSS
M7	VDDIO33	P17	VDD2	U1	TRST/	W18	VSS
M8	VSS	P19	VSS	U2	PROCMON	W19	VSS
M10	VSS	P20	VDDIO33	U3	CPCI_SWITCH	W20	VDDIO33
M11	VDD2	P21	N/C	U4	CPCI_ENUM/	W21	AD[36]
M12	VSS	P22	BWE[0]/	U5	ALT_INTA/	W22	AD[34]
M13	VDD2	P23	MCLK	U6	CPCI64_EN/	W23	AD[38]
M14	VSS	P24	MADP[2]	U7	VDDIO33	W24	MAD[30]
M15	VDD2	P25	BWE[1]/	U8	VSS	W25	MAD[22]
M16	VSS	P26	BWE[3]/	U10	VDD2	W26	MAD[28]
M17	VDD2	R1	GPIO[2]	U11	VSS	Y1	INTA/
M19	VSS	R2	VDDIO33	U12	VDD2	Y2	VDDIO33
M20	VDDIO33	R3	VSS	U13	VSS	Y3	VSS
M21	MAD[14]	R4	TDO	U14	VDD2	Y4	REQ/
M22	N/C	R5	N/C	U15	VSS	Y5	N/C
M23	PBSRAM_CS/	R6	TDI	U16	VDD2	Y6	CLK
M24	VSS	R7	VDDIO33	U17	VSS	Y7	N/C
M25	VDDIO33	R8	VSS	U19	VSS	Y8	VDDIO33
M26	MOE0/	R10	VDD2	U20	VDDIO33	Y9	VDDIO33
N1	N/C	R11	VSS	U21	N/C	Y10	VDDIO33
N2	TMS_ICE	R12	VDD2	U22	N/C	Y11	VDDIO33
N3	RTCK_ICE	R13	VSS	U23	MAD[27]	Y12	VDDIO33
N4	TRST_ICE/	R14	VDD2	U24	MAD[26]	Y13	VDDIO33
N5	TCK_ICE	R15	VSS	U25	MAD[16]	Y14	VDDIO33
N6	CPCI_LED/	R16	VDD2	U26	MAD[18]	Y15	VDDIO33
N7	VDDIO33	R17	VSS	V1	TMS		

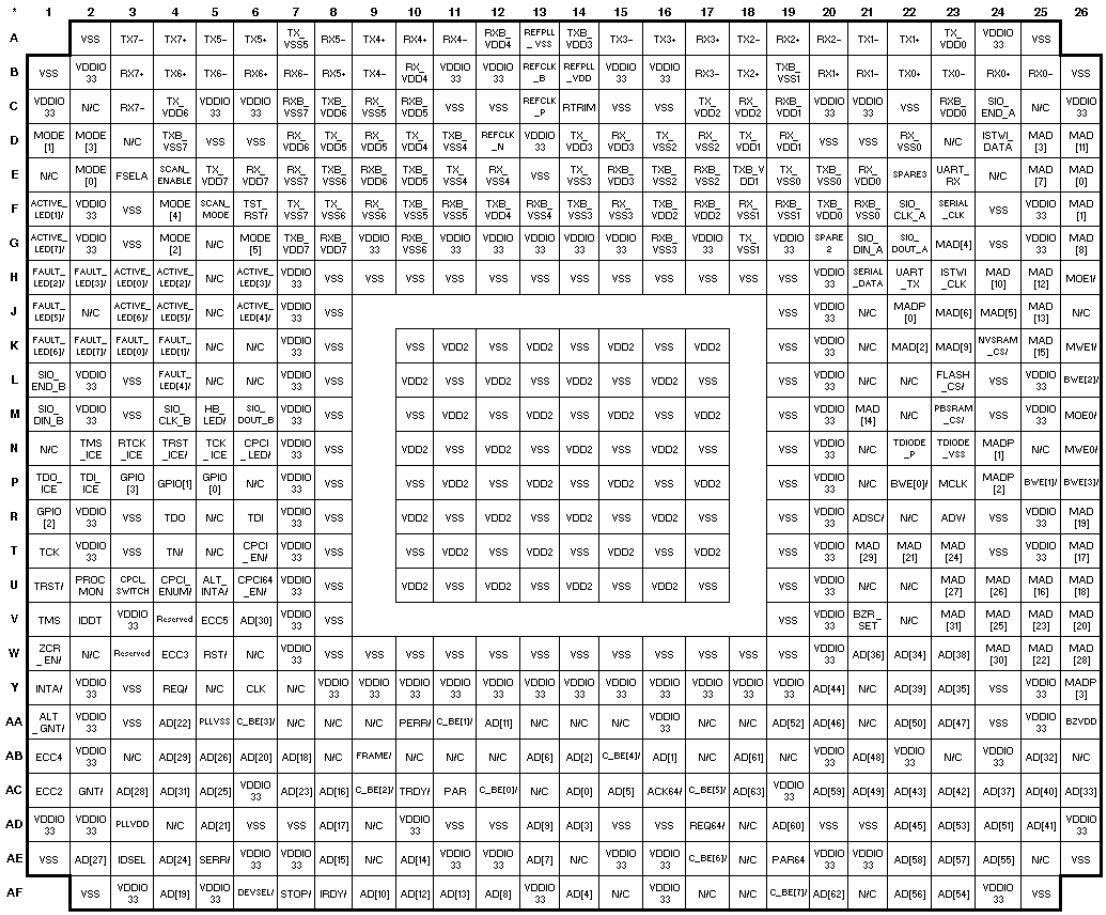
1. Pad locations marked N/C are not internally connected to the LSISAS1068 silicon. Pad locations marked RESERVED are for LSI Logic factory test use only. Refer to the Signal Description section to determine how to terminate the RESERVED pads.

Table 2 Listing by Pin Number (Cont.)[1]

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
Y16	VDDIO33	AB6	AD[20]	AC22	AD[43]	AE12	VDDIO33
Y17	VDDIO33	AB7	AD[18]	AC23	AD[42]	AE13	AD[7]
Y18	VDDIO33	AB8	N/C	AC24	AD[37]	AE14	N/C
Y19	VDDIO33	AB9	FRAME/	AC25	AD[40]	AE15	VDDIO33
Y20	AD[44]	AB10	N/C	AC26	AD[33]	AE16	VDDIO33
Y21	N/C	AB11	N/C	AD1	VDDIO33	AE17	C_BE[6]/
Y22	AD[39]	AB12	N/C	AD2	VDDIO33	AE18	N/C
Y23	AD[35]	AB13	AD[6]	AD3	PLLVDD	AE19	PAR64
Y24	VSS	AB14	AD[2]	AD4	N/C	AE20	VDDIO33
Y25	VDDIO33	AB15	C_BE[4]/	AD5	AD[21]	AE21	VDDIO33
Y26	MADP[3]	AB16	AD[1]	AD6	VSS	AE22	AD[58]
AA1	ALT_GNT/	AB17	N/C	AD7	VSS	AE23	AD[57]
AA2	VDDIO33	AB18	AD[61]	AD8	AD[17]	AE24	AD[55]
AA3	VSS	AB19	N/C	AD9	N/C	AE25	N/C
AA4	AD[22]	AB20	VDDIO33	AD10	VDDIO33	AE26	VSS
AA5	PLLVSS	AB21	AD[48]	AD11	VSS	AF2	VSS
AA6	C_BE[3]/	AB22	VDDIO33	AD12	VSS	AF3	VDDIO33
AA7	N/C	AB23	N/C	AD13	AD[9]	AF4	AD[19]
AA8	N/C	AB24	VDDIO33	AD14	AD[3]	AF5	VDDIO33
AA9	N/C	AB25	AD[32]	AD15	VSS	AF6	DEVSEL/
AA10	PERR/	AB26	N/C	AD16	VSS	AF7	STOP/
AA11	C_BE[1]/	AC1	ECC2	AD17	REQ64/	AF8	IRDY/
AA12	AD[11]	AC2	GNT/	AD18	N/C	AF9	AD[10]
AA13	N/C	AC3	AD[28]	AD19	AD[60]	AF10	AD[12]
AA14	N/C	AC4	AD[31]	AD20	VSS	AF11	AD[13]
AA15	N/C	AC5	AD[25]	AD21	VSS	AF12	AD[8]
AA16	VDDIO33	AC6	VDDIO33	AD22	AD[45]	AF13	VDDIO33
AA17	N/C	AC7	AD[23]	AD23	AD[53]	AF14	AD[4]
AA18	N/C	AC8	AD[16]	AD24	AD[51]	AF15	N/C
AA19	AD[52]	AC9	C_BE[2]/	AD25	AD[41]	AF16	VDDIO33
AA20	AD[46]	AC10	TRDY/	AD26	VDDIO33	AF17	N/C
AA21	N/C	AC11	PAR	AE1	VSS	AF18	N/C
AA22	AD[50]	AC12	C_BE[0]/	AE2	AD[27]	AF19	C_BE[7]/
AA23	AD[47]	AC13	N/C	AE3	IDSEL	AF20	AD[62]
AA24	VSS	AC14	AD[0]	AE4	AD[24]	AF21	N/C
AA25	VDDIO33	AC15	AD[5]	AE5	SERR/	AF22	AD[56]
AA26	BZVDD	AC16	ACK64/	AE6	VDDIO33	AF23	AD[54]
AB1	ECC4	AC17	C_BE[5]/	AE7	VDDIO33	AF24	VDDIO33
AB2	VDDIO33	AC18	AD[63]	AE8	AD[15]	AF25	VSS
AB3	N/C	AC19	VDDIO33	AE9	N/C		
AB4	AD[29]	AC20	AD[59]	AE10	AD[14]		
AB5	AD[26]	AC21	AD[49]	AE11	VDDIO33		

1. Pad locations marked N/C are not internally connected to the LSISAS1068 silicon. Pad locations marked RESERVED are for LSI Logic factory test use only. Refer to the Signal Description section to determine how to terminate the RESERVED pads.

Figure 4 LSISAS1068 636 EPBGA-T Diagram (Top View)



*	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A		VSS	TX7-	TX7+	TX5-	TX5+	TX_VSS5	RX5-	TX4+	RX4+	RX4-	RXB_VDD4	REFPLL_VSS	TXB_VDD3	TX3-	TX3+	RX3+	TX2-	RX2+	RX2-	TX1-	TX1+	TX_VDD0	VDDIO33	VSS	
B	VSS	VDDIO33	RX7+	TX6+	TX6-	RX6+	RX6-	RX5+	TX4-	RX_VDD4	VDDIO33	VDDIO33	REFCLK_B	REFPLL_VDD	VDDIO33	VDDIO33	RX3-	TX2+	TXB_VSS1	RX1+	RX1-	TX0+	TX0-	RX0+	RX0-	VSS
C	VDDIO33	N/C	RX7-	TX_VDD6	VDDIO33	VDDIO33	RXB_VSS7	TXB_VDD6	RX_VSS5	RXB_VDD5	VSS	VSS	REFCLK_P	RTRIM	VSS	VSS	TX_VDD2	RX_VDD2	RXB_VDD1	VDDIO33	VDDIO33	VSS	RXB_VDD0	SIO_END_A	N/C	VDDIO33
D	MODE[1]	MODE[3]	N/C	TXB_VSS7	VSS	VSS	RX_VDD6	TX_VDD5	RX_VDD5	TX_VDD4	TXB_VSS4	REFCLK_N	VDDIO33	TX_VDD3	RX_VDD3	TX_VSS2	RX_VSS2	TX_VDD1	RX_VDD1	VSS	VSS	RX_VSS0	N/C	ISTWI_DATA	MAD[3]	MAD[11]
E	N/C	MODE[0]	FSELA	SCAN_ENABLE	TX_VDD7	RX_VDD7	RX_VSS7	TXB_VSS6	RXB_VDD6	TXB_VDD5	TX_VSS4	RX_VSS4	VSS	TX_VSS3	RXB_VDD3	TXB_VSS2	RXB_VSS2	TXB_VDD1	TX_VSS0	TXB_VSS0	RX_VDD0	SPARE3	UART_RX	N/C	MAD[7]	MAD[0]
F	ACTIVE_LED[1]/	VDDIO33	VSS	MODE[4]	SCAN_MODE	TST_RST/	TX_VSS7	TX_VSS6	RX_VSS6	TXB_VSS5	RXB_VSS5	TXB_VDD4	RXB_VSS4	TXB_VSS3	RX_VSS3	TXB_VDD2	RXB_VDD2	RX_VSS1	RXB_VSS1	TXB_VDD0	RXB_VSS0	SIO_CLK_A	SERIAL_CLK	VSS	VDDIO33	MAD[1]
G	ACTIVE_LED[7]/	VDDIO33	VSS	MODE[2]	N/C	MODE[5]	TXB_VDD7	RXB_VDD7	VDDIO33	RXB_VSS6	VDDIO33	VDDIO33	VDDIO33	VDDIO33	VDDIO33	RXB_VSS3	VDDIO33	TX_VSS1	VDDIO33	SPARE2	SIO_DIN_A	SIO_DOUT_A	MAD[4]	VSS	VDDIO33	MAD[8]
H	FAULT_LED[2]/	FAULT_LED[3]/	ACTIVE_LED[0]/	ACTIVE_LED[2]/	N/C	ACTIVE_LED[3]/	VDDIO33	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIO33	SERIAL_DATA	UART_TX	ISTWI_CLK	MAD[10]	MAD[12]	MOE#/
J	FAULT_LED[5]/	N/C	ACTIVE_LED[6]/	ACTIVE_LED[5]/	N/C	ACTIVE_LED[4]/	VDDIO33	VSS											VSS	VDDIO33	N/C	MADP[0]	MAD[6]	MAD[5]	MAD[13]	N/C
K	FAULT_LED[6]/	FAULT_LED[7]/	FAULT_LED[0]/	FAULT_LED[1]/	N/C	N/C	VDDIO33	VSS		VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2		VSS	VDDIO33	N/C	MAD[2]	MAD[9]	NVSRAM_CS/	MAD[15]	MWE#/
L	SIO_END_B	VDDIO33	VSS	FAULT_LED[4]/	N/C	N/C	VDDIO33	VSS		VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS		VSS	VDDIO33	N/C	N/C	FLASH_CS/	VSS	VDDIO33	BWE[2]/
M	SIO_DIN_B	VDDIO33	VSS	SIO_CLK_B	HB_LED/	SIO_DOUT_B	VDDIO33	VSS		VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2		VSS	VDDIO33	MAD[14]	N/C	PBSRAM_CS/	VSS	VDDIO33	MOE0/
N	N/C	TMS_ICE	RTCK_ICE	TRST_ICE/	TCK_ICE	CPCI_LED/	VDDIO33	VSS		VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS		VSS	VDDIO33	N/C	TDIODE_P	TDIODE_VSS	MADP[1]	N/C	MWE0/
P	TDO_ICE	TDI_ICE	GPIO[3]	GPIO[1]	GPIO[0]	N/C	VDDIO33	VSS		VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2		VSS	VDDIO33	N/C	BWE[0]/	MCLK	MADP[2]	BWE[1]/	BWE[3]/
R	GPIO[2]	VDDIO33	VSS	TDO	N/C	TDI	VDDIO33	VSS		VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS		VSS	VDDIO33	ADSC/	N/C	ADV/	VSS	VDDIO33	MAD[19]
T	TCK	VDDIO33	VSS	TN/	N/C	CPCI_EN/	VDDIO33	VSS		VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2		VSS	VDDIO33	MAD[29]	MAD[21]	MAD[24]	VSS	VDDIO33	MAD[17]
U	TRST/	PROC_MON	CPCL_SWITCH	CPCI_ENUM/	ALT_INTA/	CPCI64_EN/	VDDIO33	VSS		VDD2	VSS	VDD2	VSS	VDD2	VSS	VDD2	VSS		VSS	VDDIO33	N/C	N/C	MAD[27]	MAD[26]	MAD[16]	MAD[18]
V	TMS	IDDT	VDDIO33	Reserved	ECC5	AD[30]	VDDIO33	VSS											VSS	VDDIO33	BZR_SET	N/C	MAD[31]	MAD[25]	MAD[23]	MAD[20]
W	ZCR_EN/	N/C	Reserved	ECC3	RST/	N/C	VDDIO33	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIO33	AD[36]	AD[34]	AD[38]	MAD[30]	MAD[22]	MAD[28]
Y	INTA/	VDDIO33	VSS	REQ/	N/C	CLK	N/C	VDDIO33	VDDIO33	VDDIO33	VDDIO33	VDDIO33	VDDIO33	VDDIO33	VDDIO33	VDDIO33	VDDIO33	VDDIO33	VDDIO33	AD[44]	N/C	AD[39]	AD[35]	VSS	VDDIO33	MADP[3]
AA	ALT_GNT/	VDDIO33	VSS	AD[22]	PLLVSS	C_BE[3]/	N/C	N/C	N/C	PERR/	C_BE[1]/	AD[11]	N/C	N/C	N/C	VDDIO33	N/C	N/C	AD[52]	AD[46]	N/C	AD[50]	AD[47]	VSS	VDDIO33	BZVDD
AB	ECC4	VDDIO33	N/C	AD[29]	AD[26]	AD[20]	AD[18]	N/C	FRAME/	N/C	N/C	N/C	AD[6]	AD[2]	C_BE[4]/	AD[1]	N/C	AD[61]	N/C	VDDIO33	AD[48]	VDDIO33	N/C	VDDIO33	AD[32]	N/C
AC	ECC2	GNT/	AD[28]	AD[31]	AD[25]	VDDIO33	AD[23]	AD[16]	C_BE[2]/	TRDY/	PAR	C_BE[0]/	N/C	AD[0]	AD[5]	ACK64/	C_BE[5]/	AD[63]	VDDIO33	AD[59]	AD[49]	AD[43]	AD[42]	AD[37]	AD[40]	AD[33]
AD	VDDIO33	VDDIO33	PLLVDD	N/C	AD[21]	VSS	VSS	AD[17]	N/C	VDDIO33	VSS	VSS	AD[9]	AD[3]	VSS	VSS	REQ64/	N/C	AD[60]	VSS	VSS	AD[45]	AD[53]	AD[51]	AD[41]	VDDIO33
AE	VSS	AD[27]	IDSEL	AD[24]	SERR/	VDDIO33	VDDIO33	AD[15]	N/C	AD[14]	VDDIO33	VDDIO33	AD[7]	N/C	VDDIO33	VDDIO33	C_BE[6]/	N/C	PAR64	VDDIO33	VDDIO33	AD[58]	AD[57]	AD[55]	N/C	VSS
AF		VSS	VDDIO33	AD[19]	VDDIO33	DEVSEL/	STOP/	IRDY/	AD[10]	AD[12]	AD[13]	AD[8]	VDDIO33	AD[4]	N/C	VDDIO33	N/C	N/C	C_BE[7]/	AD[62]	N/C	AD[56]	AD[54]	VDDIO33	VSS	

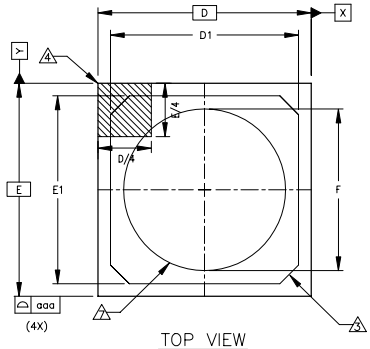
Package Drawings

The LSISAS1068 uses a 636 EPBGA-T package. The package code is 5Y. Figure 5 provides the package drawing.

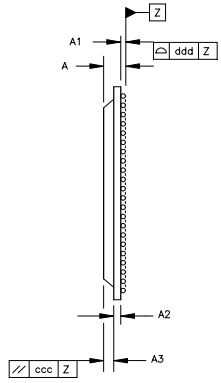
Figure 5 JZ02-000015-00 (5Y) Mechanical Drawing (Sheet 1 of 3)

REVISIONS

APPROVAL	DATE	DESCRIPTION	REV
C.FISHLEY	01–24–02	INITIAL RELEASE	0
C.FISHLEY	03–20–02	REVISE DIMENSION (ddd)	1
R.MENDOZA	01–29–03	ADD PACKAGE (4E)	2
C.FISHLEY	06–04–03	ADD PACKAGE (6i)	3
C.FISHLEY	06–25–03	ADD PACKAGE (61)	4
WK Liew	10–06–03	ADD PACKAGE (4X) (5E) (HT)	5
L. MORA	03–24–04	ADD PACKAGE (5Y)	6
WK Liew	07–02–04	ADD PACKAGE (8C)	7
C. Fishley	08–13–04	ADD PACKAGE (uo, 3w, ow, 82)	8



TOP VIEW



SIDE VIEW

TABLE 1: COMMON DIMENSIONS			
SYM	MIN	NOM	MAX
A	–	–	2.50
A1	0.40	–	–
A2	0.25	–	0.70
A3	–	–	1.25
b	0.50	–	0.70
D		27.00 BSC	
D1	23.00	–	25.00
E		27.00 BSC	
E1	23.00	–	25.00
e		1.00 BSC	
F	19.50	–	21.50

TABLE 2: TOLERANCES OF FORM AND POSITION	
DIMENSION	e = 1.00
aaa	0.20
ccc	0.35
ddd	0.15
eee	0.25
fff	0.10

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. ALL DIMENSIONS IN MM.
3. CORNER DETAIL IS LSI LOGIC CORPORATION OPTION.
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, AND MAY CONSIST OF INK, LASER MARK OR METALLIZED MARKING, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
5. JEDEC CODE MS–034.
6. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. HEAT SPREADER OUTLINE.

LSI LOGIC CORPORATION
1551 McCARTHY BLVD. MILPITAS, CA. 95035

TITLE: 27x27mm EPBGA–T, EPBGA–HP 1.00 BALL PITCH

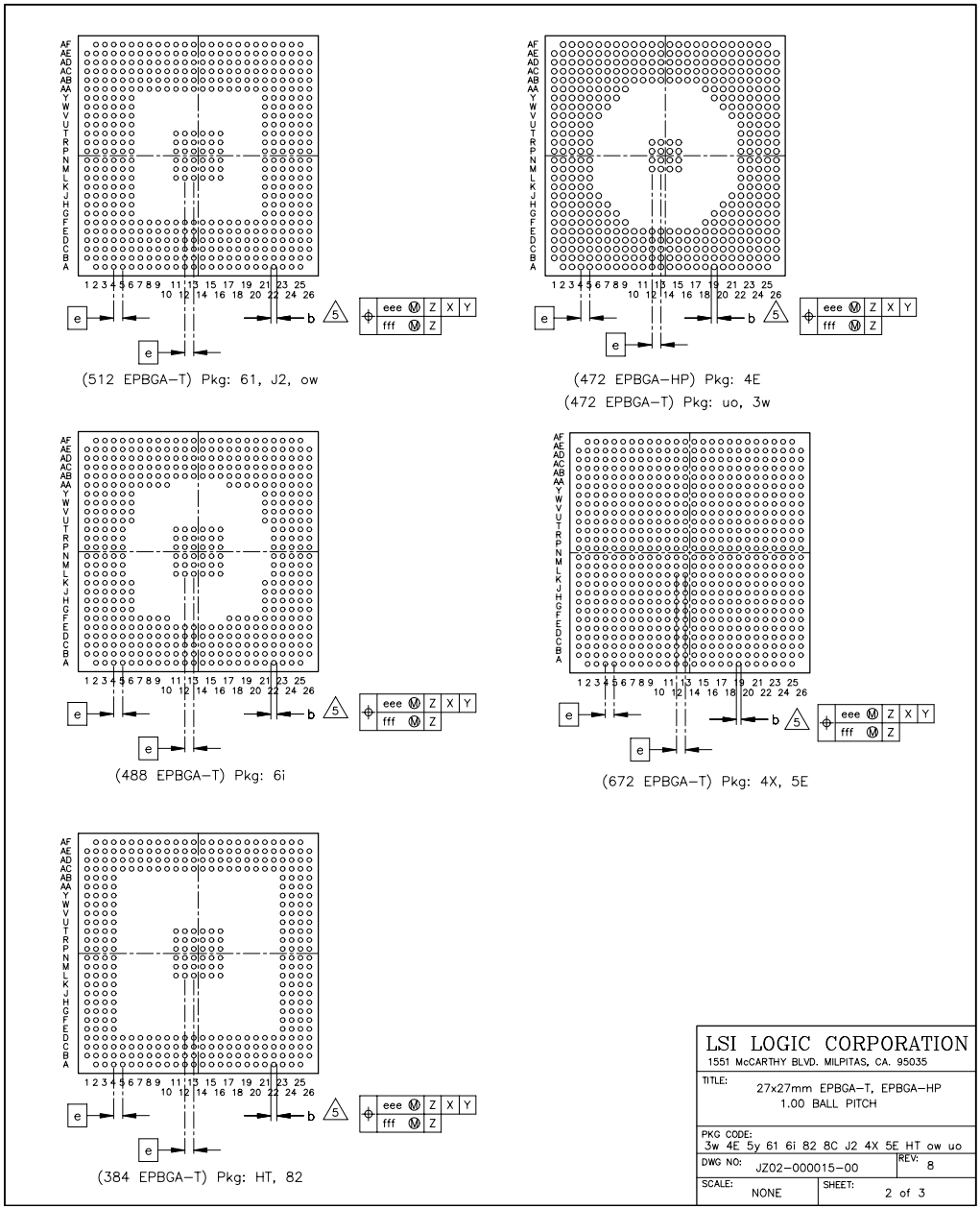
PKG CODE: 3w 4E 5y 61 6i 82 8C J2 4X 5E HT ow uo

DWG NO: JZ02–000015–00 REV: 8

SCALE: NONE SHEET: 1 of 3

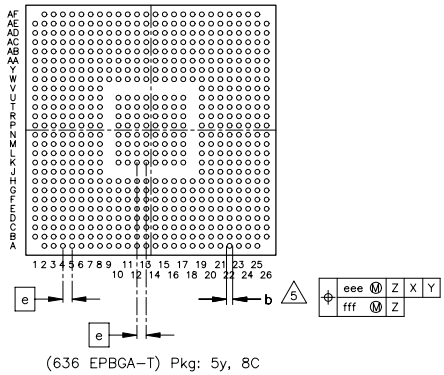
Important: **For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code 5Y.**

Figure 5 JZ02-000015-00 (5Y) Mechanical Drawing; Bottom View (Sheet 2 of 3)



Important: **For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code 5Y.**

Figure 5 JZ02-000015-00 (5Y) Mechanical Drawing; Bottom View (Sheet 3 of 3)



LSI LOGIC CORPORATION 1551 McCARTHY BLVD. MILPITAS, CA. 95035	
TITLE: 27x27mm EPBGA–T, EPBGA–HP 1.00 BALL PITCH	
PKG CODE: 3w 4E 5y 61 6i 82 8C J2 4X 5E HT ow uo	
DWG NO: JZ02–000015–00	REV: 8
SCALE: NONE	SHEET: 3 of 3

Important: **For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code 5Y.**

Notes

Notes

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AP/DB
Printed in USA

Doc. No. DB08-000240-04

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