

PowerPCTM 970:

First in a new family of 64-bit high performance PowerPC processors



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PowerPC 970 Design Objectives and Overview **PowerPC**



- Leverage architectural advantages of 64-bit POWER4[™] for new generation of PowerPC processor
- Provide high performance general purpose processing through advanced superscalar design with multiple, pipelined execution units
- Enhance multimedia, graphics and data movement through hardware implementation of a SIMD processing facility
- Support the bandwidth demands of a highly superscalar and SIMD enhanced core through a high speed processor bus



IBM PowerPC High Performance Roadmap

64-Bit Microprocessors PowerPC 970

PPC 970 1.4 – 1.8 GHz

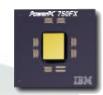
32-Bit Microprocessors



PPC 750 300 - 500MHz



PPC 750CXe 300 - 600MHz



PPC 750FX 500 - 1000MHz



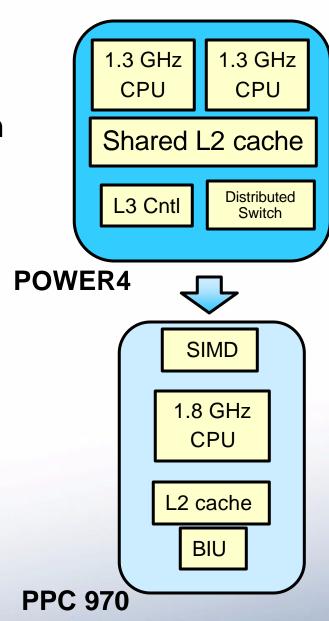




Based on POWER4 Architecture



- Winner MPR analyst's choice, 2001
- POWER4 design goals
 - Balanced system/bus throughput design
 - SMP optimization
 - Native 32-bit compatibility
 - High frequency
- PPC 970 implementation
 - SIMD enhanced
 - Lower power
 - Smaller die
 - Single processor core

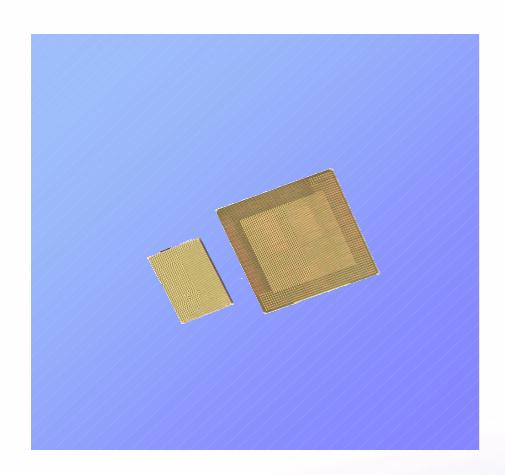


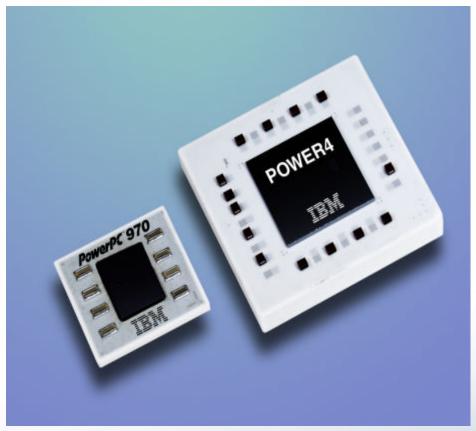


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PPC 970 / POWER4 Size Comparison









PPC 970 Features



Instruction pipe

- 64KB L1 Inst cache, direct mapped
- 32 entry I buffer
- 8 instructions fetch / cycle

Branch prediction

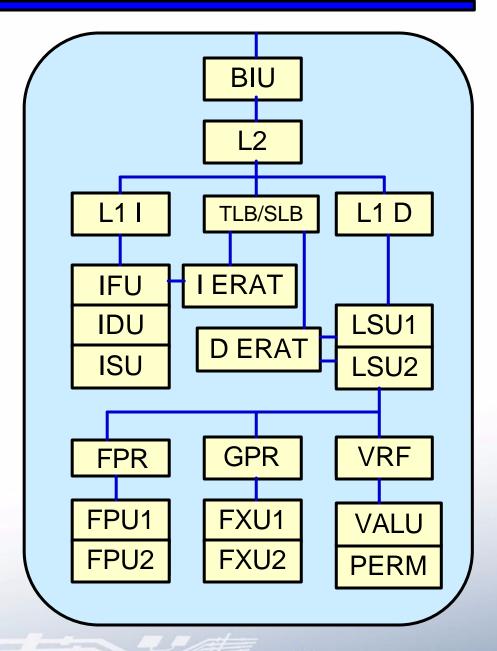
Highly accurate dynamic prediction

Dispatch, issue

- 1 group (4 + branch) / cycle
- Up to 20 active groups
- Up to 8 issue / cycle
- Over 200 instructions in flight

Data pipe

- 32 KB L1 Data cache, 2-way sa
- 32 x 64b GPR, FPR
- 32 x 128b VRF
- 512KB L2 cache, 8-way sa
- 8 data prefetch streams





PPC 970 Features (cont.)

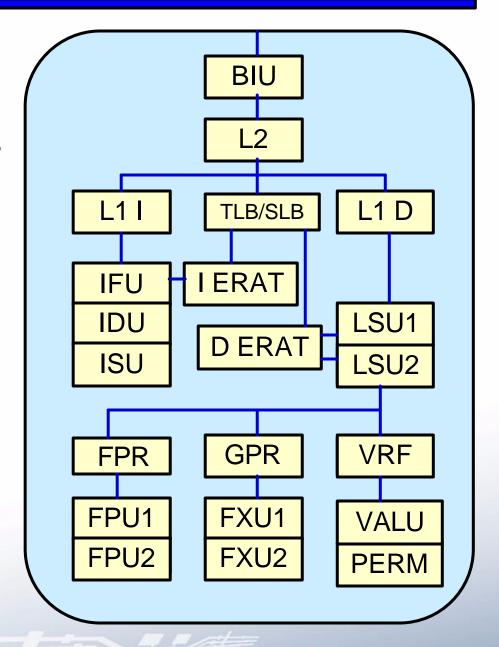


Memory management

- 64 entry SLB, fully associative
- 256 x 4-way TLB
- 64 x 2-way Inst and Data ERATs
- Supports 42-bit real addresses

Execution

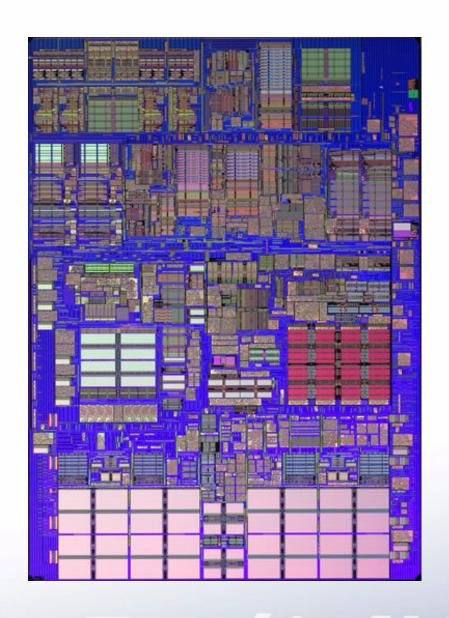
- 2 Load/store units
 - 64b for GPR, FPR
 - 128b for VRF
- 2 Fixed point units
- 2 IEEE floating point units
 - Single-, double-precision
- 2 SIMD sub-units
 - VALU 2 integer, float subunits
 - VPERM permute
- Branch unit
- Condition register unit





PowerPC 970 Die Overview







PPC 970 Pipeline



Pipeline depths

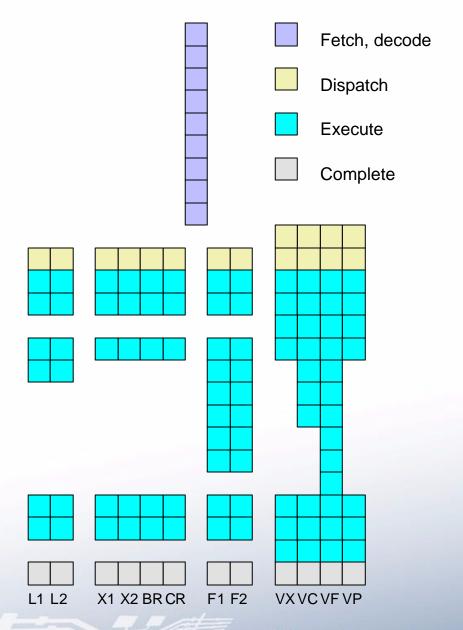
- 9 fetch, decode stages
- 5 to 13 out of order execute stages
- 2-3 dispatch, completion stages

Pipeline width

- Up to 8 fetched per cycle
- Up to 5 dispatched per cycle
- Up to 8 issued per cycle
- 12 execution units
- Up to 8 L1 D cache misses
- Up to 5 completed per cycle

Branch prediction

- Up to 2 branches per cycle
- 3 16K x 1 BHTs
- Link stack, count cache





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64-bit Processing - 32-bit Compatibility



64-bit advantages

- Driven by need to address larger memory spaces
- Performance advantage for data intensive applications
- Enable new 64-bit solutions

Native 64-bit mode

- 64-bit fixed point processing
- 64-bit effective addresses
- 42-bit real addresses
- Segment lookaside buffer caches segment table entries

Native 32-bit mode

- High word of all effective addresses are cleared
- 32-bit PPC application code supported
- First 16 entries of SLB are used as segment registers

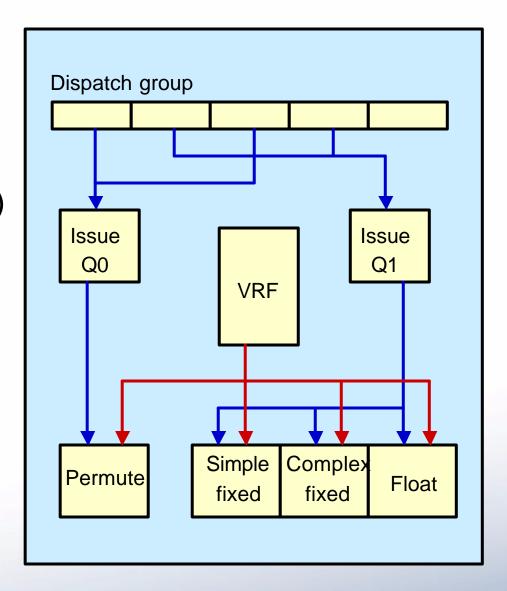


SIMD/Vector Engine



Features

- 162 specialized SIMD instructions
- 128-bit data paths
- 4-way SIMD single precision floating point (8 FP ops/cycle)
- 4-way, 8-way, 16-way SIMD fixed point operations
- Two execution units
 - Permute unit
 - 16-entry issue queue
 - Permute, splat, merge
 - ALU 3 subunits
 - 20-entry issue queue
 - Simple, complex fixed point
 - Floating point



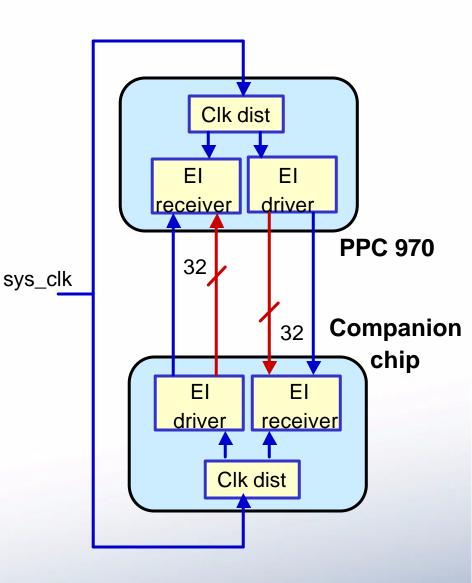


High Bandwidth Processor Bus



Features

- Two unidirectional busses
- 32-bit read, 32-bit write
- Point-to-point
- Source synchronous
- Elastic interface
 - Allows multiple cycle wire delays between chips
 - Hardware deskews bit lines at POR
- Bus protocol
 - Address, control and data multiplexing
 - Sideband signals for snoop and ACK
 - Pipelined transactions
 - Out of order data
 - Coherency and sharing via snooping
 - Processor synchronization for SMP
- Up to 900 MHz bit rate achieves up to 6.4 GB/s useable bandwidth





PPC 970 Performance



SPECint2000

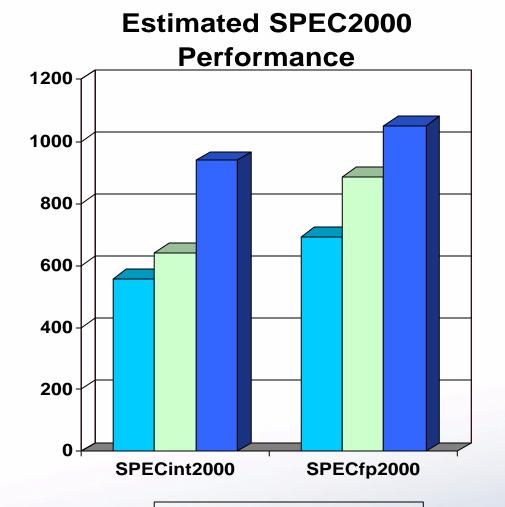
- 937 @ 1.8 GHz*
- SPECfp2000
 - 1051 @ 1.8 GHz*

Dhrystone MIPS

- 5220 @ 1.8 GHz*
- 2.9 DMIPS / MHz

Additional Performance

- Peak scalar GFLOPS = 7.2
- Peak SIMD GFLOPS = 14.4
- RC5 : 18M keys/sec*



- PPC 970 @ 1.0 GHz
- □ POWER4 @ 1.0 GHz
- PPC 970 @ 1.8 GHz



PowerPC 970 Parametrics



Target Frequencies	1.4 to 1.8 GHz
Architecture	64-bit PowerPC, 32-bit compatible
Performance*	937 SPECint2000 @ 1.8 GHz 1051 SPECfp2000 @ 1.8 GHz 5220 DMIPS @ 1.8 GHz (2.9 DMIPS/MHz)
Caches	64KB, I cache, w/parity 32KB, D cache, w/parity 512KB, L2 cache, w/ECC
Voltages	1.3V core logic and I/Os
Typical Power Dissipation*	42W @ 1.8 GHz, 1.3v 19W @ 1.2 GHz, 1.1v
Package	25x25mm CBGA 576 pins on 1mm pitch (161 signals)
Technology	0.13mm, CMOS w/ SOI 8 levels of copper interconnect
Target Schedule*	Samples 2Q 2003, Production 2H 2003



*Estimation only; subject to change without notice.

Target frequencies are subject to change without notice.

Any performance data contained herein is preliminary and subject to change.

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Conclusion



The IBM PowerPC 970 design constitutes

- An advanced 64-bit processor
- Derived from the POWER4 core
- Enhanced by a SIMD/Vector engine
- With a high bandwidth memory bus
- To achieve high performance on compute and bandwidth intensive applications



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